Field Dependent Self-Heating Effects in High-Power AlGaN/GaN HEMTs

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Abstract

In this work, we investigate the self-heating behaviour of high-power AlGaN/GaN HEMTs. Micro-Raman thermography measurements were carried out to determine the device temperature at different power and applied voltage levels. We found that drain voltage influences the device temperature distribution when the dissipated power is kept constant by applying a gate bias. This effect was then investigated and explained by use of numerical electro-thermal device simulations.

INTRODUCTION

Thermal management of power devices is one of the key issues in reliability considerations especially for high power devices like AlGaN/GaN HEMTs. Poor reliability of GaN-based devices is very often a consequence of an excessive and localized channel temperature rise. Knowledge of the actual thermal resistance of such devices is therefore essential for the improvement of their reliability. The self-heating of power devices has been studied by various groups either by experimental methods [1] or numerical simulations assuming a localized heating area with a heat power density coming from the dissipated DC power density of the device under operation. On the other hand, degradation often increases with increasing drain voltage as also stated in [2]. We show that considering the dissipated DC power density alone is not sufficient to accurately predict the device temperature because drain voltage influences the device temperature distribution at constant power level.

CHARACTERIZATION AND SIMULATION

Micro-Raman thermography measurements were performed on AlGaN/GaN HEMTs fabricated by MOCVD on 4H-SiC substrate to determine their device temperature at various power levels and drain-source voltages (V_{DS}). More details on Raman thermography can be found in [3] and [4]. The epitaxy is unintentionally doped except the deep acceptor counter doping in the GaN buffer layer. The fabrication process utilizes a dielectric assisted gate process with an asymmetrically aligned gate with a Γ-gate with L_G=500nm, 500nm and 300nm of Γ-gate overhang to the drain and source, respectively. Ohmic contacts are based on Ti/Al/Ni/Au/Pt and the source-gate and gate-drain distances are 1.5µm and 4.0µm, respectively.

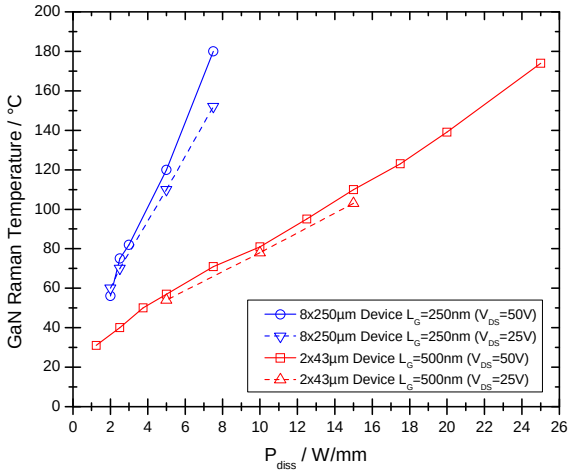

Figure 1: Results of micro-Raman thermography measurements on an 8x250µm device with L_G=250nm and a 2x43µm device with L_G=500nm. The effect is more pronounced at a higher number of gate-fingers, which results in a higher temperature difference even at lower DC power level.

The average GaN layer temperatures near the drain side of the gate for an 8x250µm device with L_G=250nm and a 2x43µm device with L_G=500nm, respectively, are plotted in Figure 1 versus the dissipated DC power density for drain voltages of V_{DS}=25V and V_{DS}=50V. We observe consistently higher GaN temperatures for higher bias voltages, although the dissipated power is constant. To understand this phenomenon we performed 2-dimensional numerical devices simulations using Silvaco ATLAS [5], which utilizes an electro-thermal model based on the drift-diffusion carrier transport equations. Figure 2 shows the simulated 2-dimensional temperature map for a dissipated power level of P_{diss}=13.5W/mm at V_{DS}=50V. In Figure 3 the simulated profile along the channel and at a depth of 1µm in the GaN buffer for a dissipated power level of P_{diss}=13.5W/mm at V_{DS}=50V is compared to the profile for the same power density at V_{DS}=25V. It is apparent that while maximum channel temperatures are comparable, at 50V bias

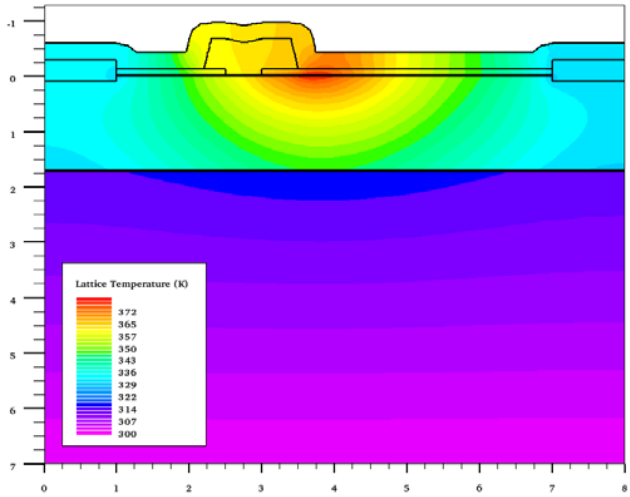

Figure 2: Simulated 2-dimensional temperature profile map for a dissipated power level of P_{diss}=13.5W/mm at V_{DS}=50V.

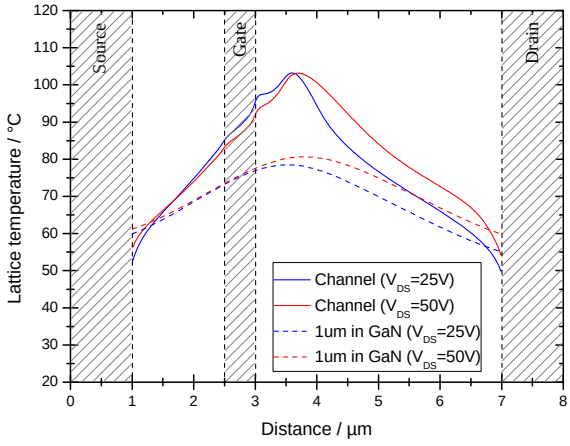

Figure 3: Simulated temperature profile along the channel and at a depth of 1µm in the GaN buffer for a dissipated power level of P_{diss}=13.5W/mm at V_{DS}=25V and V_{DS}=50V.

the temperature profile becomes broader and more asymmetric towards the drain side resulting in about 10%-higher temperature in the gate-drain region, where the micro-Raman measurements are taken. The first important observation from the simulation results is the shift of the hot-spot towards the drain with increasing drain voltage, as shown by the simulated location of the hot-spot as a function of the applied drain voltage in Figure 4. Secondly, once the hot-spot has reached the edge of the Γ-gate overhang at high bias, the shift of hot-spot location becomes less pronounced once again. Figure 4 also shows that the shift of the hot-spot in the device is influenced by the density of surface traps n_{it}. These surface traps are located at the interface between semiconductor and passivation. The simulation data shows that the shift of the hot-spot becomes less with increasing trap density. This is due to the fact that the electric field under the Γ-gate drastically increases with increasing trap

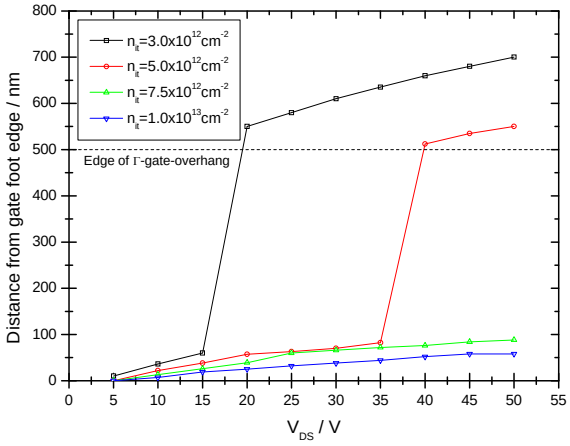

Figure 4: Simulated position of the hot spot in the channel versus the applied drain voltage indicated by the distance from the gate foot edge.

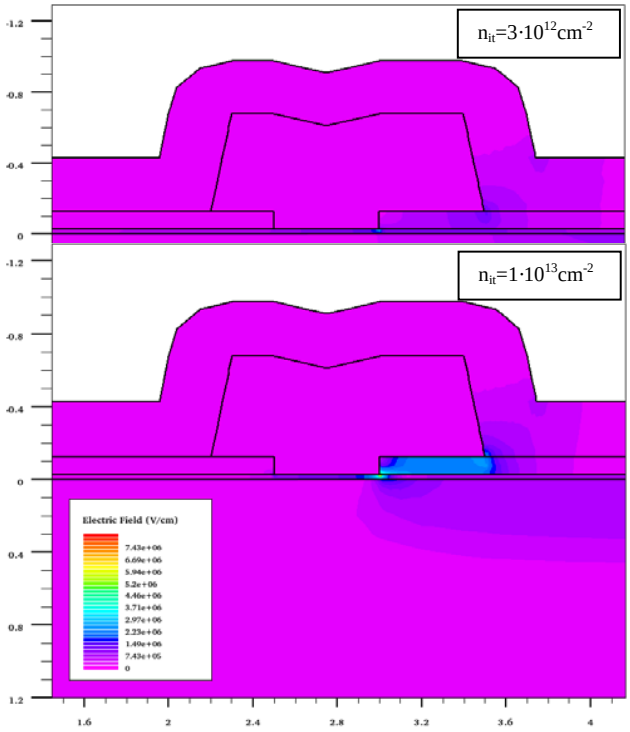

Figure 5: Simulated electric field distribution at a bias point of V_{GS}=0V and V_{DS}=50V for surface trap densities of $n_{it}=3\cdot10^{12}cm^{-2}$ and $n_{it}=1\cdot10^{13}cm^{-2}$.

density which lead to a strong localization of the field peak close to the gate contact as depicted in Figure 5. According to [6], [7] and [8] normal trap densities for passivated device are in the range of $n_{it}=2\cdot10^{12}cm^{-2}\ldots5\cdot10^{12}cm^{-2}$ whereas a density in the order of $n_{it}=1\cdot10^{13}cm^{-2}$ is usually observed only in unpassivated devices. From these results we can conclude that for reasonable densities $n_{it}<7.5\cdot10^{12}cm^{-2}$ in case of passivated devices a significant shift can be observed. However, this effect does not fully explain the observed and simulated temperature variation at different

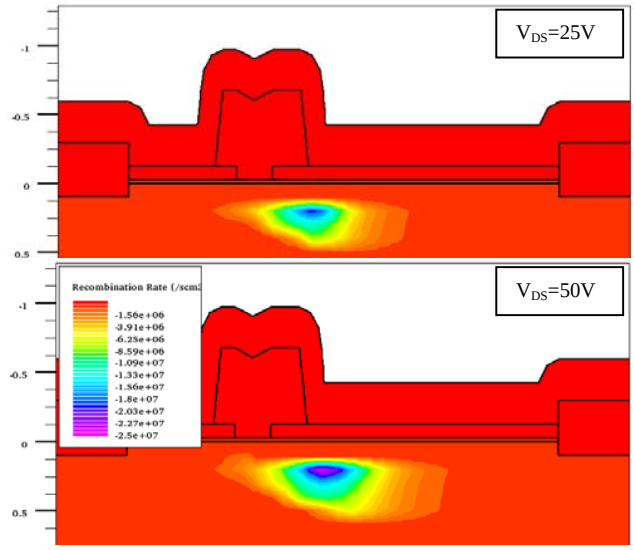

Figure 5: Simulated electron recombination rates under operation at V_{DS}=25V and V_{DS}=50V for P_{diss}=13.5W/mm.

bias levels because the observed temperature difference due to the hot-spot shift would be still too small compared to the measurement data. A more significant contribution comes from a strong increase in the electron recombination rate in the gate-drain region with increasing electric field as a consequence of the higher applied drain voltage. This effect can be seen in the simulation results depicted in Figure 5 where a 2-dimensional map of the recombination rate is shown for V_{DS}=25V and V_{DS}=50V, respectively, at the same dissipated power levels. With increasing bias voltages not only the recombination rate becomes higher but also the region of high recombination rate extends more towards drain-side of the channel. Each recombination process in the device generates a phonon which leads to a local temperature rise of the lattice. Therefore the higher and more extended region of high recombination rate contributes to an additional temperature rise and a broader temperature profile in the gate drain region.

CONCLUSIONS

We have found that the applied drain voltage influences the self-heating and temperature distribution of AlGaN/GaN HEMTs, even when power dissipation remains constant. Numerical electro-thermal device simulations showed that this is a consequence of the higher electric field in the gate-drain region which can be strongly influenced by the density of surface traps in the device resulting in a higher electron recombination rate in combination with a shift of the hot-spot in the device towards the drain side with increasing drain bias. This leads to a higher temperature in the gate-drain region whereas the maximum channel temperature remains relatively unaffected. This was in good agreement with experimental results by Raman spectroscopy.

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ACRONYMS

HEMT: High Electron Mobility Transistor
(Al)GaN: (Aluminum) Gallium Nitride
SiC: Silicon Carbide
MOCVD: Metal-Organic Chemical Vapor Deposition