

# Thermal and Piezoelectric Stress in Operating AlGaIn/GaN HFET Devices and Effect of the Fe Doping in the GaN Buffer Layer

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## Abstract

We investigated the effect of self-heating and applied source-drain voltage ( $V_{ds}$ ) on the mechanical strain/stress generated in operating AlGaIn/GaN HFET devices. Strain/stresses in devices were probed using Raman optical spectroscopy and the data were compared with electrical and thermo-mechanical numerical modeling. The vertical electric field and related piezoelectric stress near the drain-gate region were found to be significantly influenced by applied voltage and doping in the buffer. A higher level of buffer doping increases the piezoelectric stress in the AlGaIn/GaN interface, i.e., 2DEG channel region. On the other hand, the determined thermal stress generated by non-uniform self-heating is opposite in sign to the piezoelectric stress and can result in a reduction of the net stress in the operated device.

## INTRODUCTION

Since short and long term reliability of the GaN based RF devices still remains the major challenge for this promising wide bandgap technology, the main goal of this work was to study the effect of applied voltage and non-uniform self-heating on generation of mechanical strain or stresses in operating AlGaIn/GaN devices. It was shown in previous works [1-3], that applied voltage generates converse piezoelectric stress in operating AlGaIn/GaN devices, and was suggested to be responsible for device degradation via formation of defects in the AlGaIn layer and trap centers near the gate, which affects device RF performance and can ultimately also result in device failure. However, the role of thermal stresses arising from non-uniform heating is less studied and there is very limited knowledge on its effects for AlGaIn/GaN devices.

## EXPERIMENTAL DETAILS AND METHODS.

AlGaIn/GaN HFET devices were studied grown by MOCVD on the semi-insulated SiC substrate using 1.3  $\mu\text{m}$  undoped (unintentionally doped) GaN buffer, or 1.9  $\mu\text{m}$  GaN buffer with different acceptor doping levels using *in-situ* Fe doping. Device fabrication was similar to our

previous studies and details of doping and device layer structure can be found elsewhere [1,4]. The HFET devices studied had a 5  $\mu\text{m}$  source-drain gap and gate had 1.2  $\mu\text{m}$  length and 50-100  $\mu\text{m}$  width. In addition to these, mesa isolated structures with contact separation of 28  $\mu\text{m}$ , similar to a standard TLM design, on the same wafers were used for high voltage measurements, since stable pinched-off operation was limited below 40V source-drain bias in our HFET devices.

To extract the strain and stress caused by localized self-heating in the device structure and applied electric field, i.e., thermal and piezoelectric stresses respectively, spatially resolved micro-Raman measurements were performed on the operating devices. Stress induced frequency shifts of the  $E_2$  and  $A_1(\text{LO})$  phonon modes averaged through whole GaN buffer thickness were monitored. Piezoelectric stress in the devices was extracted from phonon frequency shifts in pinched-off state, and thermal stress is estimated from the directional anisotropy of phonon mode frequencies induced by non-uniform self-heating in devices. More details about the technique can be found in [1].

For 2D electrical simulations a finite-element ATLAS/BLAZE package was used, with net acceptor concentration of  $3 \times 10^{16} \text{ cm}^{-3}$  assumed in the undoped GaN buffer. For the Fe doped samples doping profiles from Ref. 4 were assumed. Numerical 3D thermo-mechanical simulations are performed using TAS finite-difference code.

## RESULTS AND DISCUSSION.

Applied  $V_{ds}$  bias generates tensile in-plane stress in the device via the converse piezoelectric effect, related to the presence of the vertical electric field in the device structure.[1] This vertical electric field is associated with the reverse biased depletion region in the GaN buffer near drain-gate area, and this is where the piezoelectric stress is generated. Assuming full mechanical clamping of GaN layer to the SiC substrate, generated in-plane piezoelectric stress  $\sigma_{xx}$  should be directly proportional to the measured phonon shift or vertical electric field magnitude. Analysis of measured stress induced phonon shift dependence on the applied  $V_{ds}$  (Fig. 1a) reveals that below 40V phonon shift

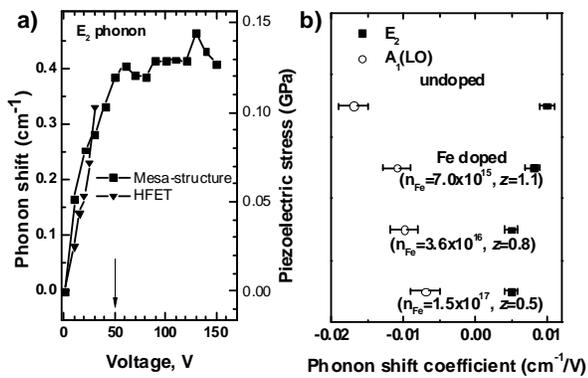


Fig. 1. a) Phonon shift and related piezoelectric stress induced by an applied drain bias in AlGaIn/GaN HFET (below 40V) and mesa-isolated structure. Arrow indicates saturation voltage. b) Coefficients of phonon frequency change per applied bias ( $V_{ds} \leq 30$  V) for the phonon modes in AlGaIn/GaN HFET devices with undoped and Fe-doped GaN buffer.

and stress are linearly dependent on the voltage, which agrees with our earlier observations [1]. However, above ~50V a saturation behavior of the electric field and stress in the GaN buffer was observed (Fig. 1a). The results of numerical simulation of the device electric field showed that for voltages higher than 50V undoped GaN buffer is almost completely depleted in the drain-gate region, which explains the saturation behavior of the observed phonon shift with applied drain voltage.

Doping of the buffer layer with Fe, which is widely used to improve control of short-channel effects in HFETs [4], has a pronounced effect on the electric field distribution in the device. Doping with Fe raises the acceptor concentration and hence decreases the depletion width in the GaN buffer. Numerical simulations predict that in such doped devices the vertical electric field and hence the piezoelectric strain/stress are almost entirely confined to the AlGaIn/GaN interface, i.e., in the 2DEG channel region, in contrast to the devices with undoped buffer, where electric field and strain are spread through the whole buffer layer thickness. Such stress concentration at the interface can be experimentally observed in Raman measurement through a reduced phonon shift coefficient per bias voltage (Fig. 1b), as for Fe doped devices most of the GaN buffer is not affected by the piezoelectric strain/stress resulting in a smaller voltage phonon shift coefficient per applied voltage. Concentration of piezoelectric strain/stress at the AlGaIn/GaN interface from additional doping in the buffer also dramatically increases the magnitude of a peak electric field from 0.7 MV/cm (undoped) to about 2.4 MV/cm (Fe doped) at 40V bias. This has a potentially negative impact on device reliability, as pinched-off stressing reliability studies show [2,3].

At the same time, during device operation highly localized self-heating related to the peak lateral electric field near the drain-side of the gate contact produces a non-uniform temperature distribution in the device, which in turn gives rise to the compressive thermal strain/stress (Fig. 2, inset). As device length is often much smaller than device

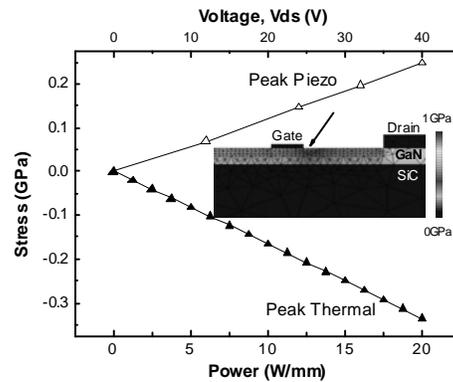


Fig. 2. Peak converse piezoelectric and thermal stresses near the drain edge of the gate contact at the AlGaIn/GaN interface in an undoped HFET device as a function of drain voltage/ dissipated power level. Inset shows a section of calculated distribution of the thermo-mechanical stress for the HFET device and location of peak stresses (arrow).

width this stress is highly anisotropic in the GaN basal plane. Combining measured by Raman spectroscopy anisotropy in thermal stress and finite-difference simulations the peak thermal stress values near the AlGaIn/GaN interface (Fig. 2) were extracted. For the devices studied here we found that piezoelectric and thermal stresses in the HFET are opposing each other in sign and are on the same order of magnitude. As a result this is likely to cause lower net stress near the drain-side gate region in the operating device, compared with pinched-off stressing, and can at least partially be responsible for the previously observed slower device degradation in the on-state [3].

## CONCLUSIONS

Optical Raman spectroscopy measurements were performed to study the effect of self-heating and applied source-drain voltage on the mechanical strain/stress generated in operating AlGaIn/GaN HFET devices. Converse piezoelectric stress was found to be significantly influenced by applied drain voltage. Additionally, the acceptor doping in the buffer was demonstrated to increase the magnitude electric field/piezoelectric stress in the AlGaIn/GaN interface region, i.e., in the device channel, leading potentially to a higher risk for device degradation. Thermal stress related to a non-uniform self-heating was determined to be opposite in sign to the piezoelectric stress and can result in reduction of the net stress in the on-state operated devices.

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