A Foundry-Ready Ultra High f_T InP/InGaAs DHBT Technology

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Abstract

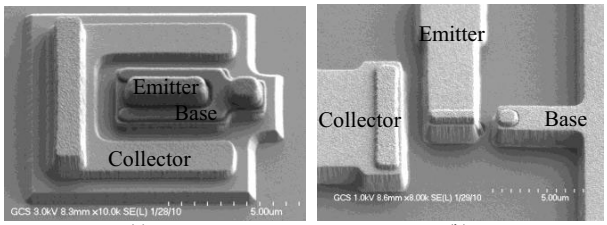
An ultra-high-f_T InP/InGaAs DHBT technology has been developed and qualified for foundry service. The device has f_T of up to 300GHz, f_{max} > 250GHz, and is very reliable, with MTTF >2x10^6 hours at Tj of 125^{o}C. This technology is an ideal candidate for high-speed digital, millimeter-wave and mixed-signal circuits. Tradeoffs between f_T and BVceo have been studied and advantages of InP DHBT over InP SHBT and SiGe HBT are reported in this paper.

INTRODUCTION

InP/InGaAs HBT is an excellent electronic device for optical communication systems and high-frequency test instruments due to its high speed and low power consumption. InP HBTs with f_T >150GHz have been used as foundry process to manufacture high-speed products at GCS for several years [1]. Although they can meet current 40 to 50Gbps applications, there are demands for higher speed and higher bit rate applications such as cloud computing, which require ultra high f_T devices, and some millimeter-wave circuits that require decent breakdown voltage and good threshold voltage control. InP based HBTs are good candidates for these applications. There are several reports of InP/InGaAs [2] and InP/GaAsSb [3] HBTs with f_T >300GHz, but they typically require operating current density of >500kA/cm^2 in order to achieve the reported high f_T. This high current density would raise the device junction temperature to such a high level that could cause reliability concerns. InP DHBT for 100Gbps application has been demonstrated, but no reliability data were reported [4]. Moreover, these advanced InP HBT processes are not available for open foundry services. In this paper, we report ultra-high-f_T InP/InGaAs DHBTs with f_T of up to 300GHz and MTTF >2x10^6 hours at Tj of 125^{o}C. This technology is readily available for foundry services with a reliability report and a complete design kit.

DEVICE FABRICATION

The ultra-high-f_T InP DHBT epi structures consist of an InP emitter, a thin carbon-doped InGaAs base, and an InP collector structure with a grading layer between InGaAs base and InP collector to eliminate electron blocking. Two DHBT structures (DHBT2 with f_T of 250GHz and DHBT3 with f_T of 300GHz) with different collector thickness were designed and fabricated. The key process steps include self-aligned emitter metal/emitter mesa, non-self-aligned base metal, base mesa, collector metal, and collector mesa. Metal posts on base and collector metals are used to make their heights at the same level as that of emitter metal. BCB is used for device passivation and planarization. BCB etch-back process is employed to expose emitter, base and collector posts for the first-level metal to access those three contacts. BCB is also used as low-loss interlayer dielectric between first and second level metals. TaN TFR and Si_3N_4 MIM capacitor are used for monolithic integration of passive components. Backside through-substrate via with low-inductance grounding is available to further enhance the circuit performance and design flexibility. All InP HBT processes are on 4-inch wafers. Standard HBT emitter sizes are 0.8x3μm^2, 0.8x6μm^2, and 0.8x10 μm^2. Fig. 1 shows the SEM pictures of a 0.8x3μm^2 DHBT (a) prior to BCB passivation and (b) posts and first-level interconnect metal.



(a) (b)

Figure 1. SEM pictures of a 0.8x3μm^2 DHBT, (a) prior to BCB passivation, (b) posts and first level interconnect metal.

DEVICEPERFORMANCE

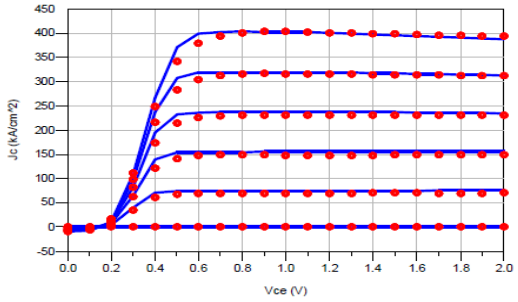


Figure 2. Typical IV curves of a 0.8x5 μm^2 InP DHBT3 device. Solid lines are measured data and dots are modeled data.

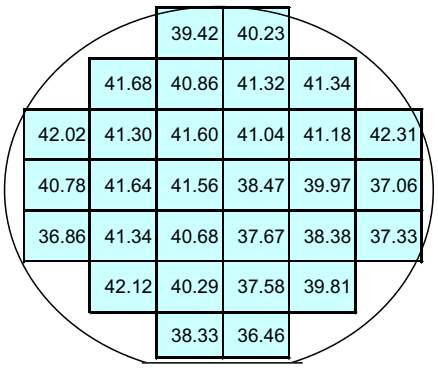


Figure 3. Typical current gain wafer map of a 0.8x3 μm^2 DHBT3 at Jc =100kA/cm^2.

Fig. 2 shows the typical IV curves of a 0.8x5 μm^2 DHBT3 device. The Vce offset voltage is 0.15V, and the knee voltage is 0.5V at Jc =300kA/cm^2, which are similar to those of an SHBT, indicating that there is no electron blocking effect in the base-collector heterojunction. The typical current gain is ~40 at Jc of 100 kA/cm^2 for both DHBT2 and DHBT3. Fig. 3 shows a typical wafer map of the current gain distribution for a 0.8x3 μm^2 DHBT3 at Jc =100kA/cm^2 on a 4-inch wafer.

On-wafer small-signal RF performance was measured with vector network analyzer from 0.5 to 40GHz. Fig. 4 shows the measured |H21| and maximum stable/available gain, MSG/Gmax, as functions of frequency. f_T and f_{max} are extrapolated by using a –20dB/decade slope. Due to frequency limitation of our test equipment, the onset of maximum available gain is beyond 40GHz and the extrapolated f_{max} value of 250GHz at Jc =300kA/cm^2 may be underestimated. Fig. 5 shows f_T vs. Jc at Vce=1.0V, 1.5V, and 2.0V of a DHBT3 device. f_T reaches 290GHz and 300GHz at Vce=1.0V, Jc =300 and 400kA/cm^2, respectively.

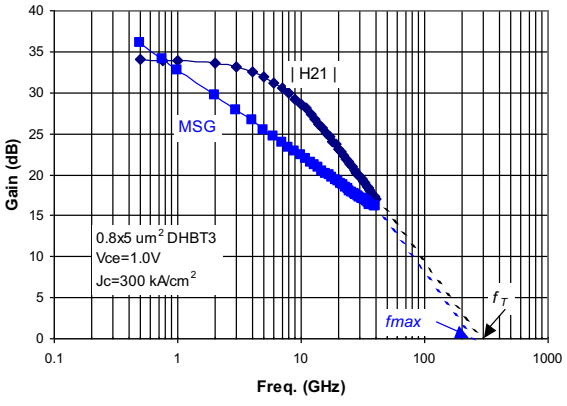


Figure 4. |H21| and MSG/Gmax vs frequency for a 0.8x5 μm^2 InP DHBT3 device at Vce=1.0V and Jc =300kA/cm^2.

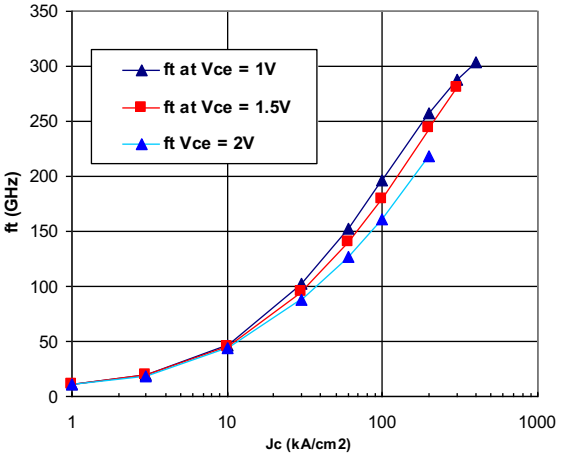


Figure 5. f_T vs Jc for a 0.8x5 μm^2 InP DHBT3 device at Vce = 1.0, 1.5, and 2.0V at room temperature.

To provide optimum performance for different applications, tradeoffs between f_T and $BVceo$ have been studied. Both SHBTs and DHBTs with different collector structures were designed and fabricated for comparison. Fig. 6 shows f_T vs $BVceo$ for InP DHBTs and InP SHBTs with different collector thickness designs. A SiGe HBT data [5] is also included as reference. Although $BVceo$ is affected by current gain and collector doping, it is mainly determined by the collector thickness and band-gap. If we use $f_T \bullet BVceo$ as the figure of merit (FOM), it is clearly shown that DHBT offers the best FOM. Since the InP DHBTs of this work are aimed for high-speed digital, millimeter-wave, and mixed-signal applications, $BVceo$ of >3.5V can meet the requirement for most of the applications. In comparison, $BVceo$ of InP SHBT is about 1.7V lower than that of DHBT with the same f_T. Therefore, DHBTs have been chosen for foundry services to provide a higher breakdown voltage while maintaining ultra high f_T.

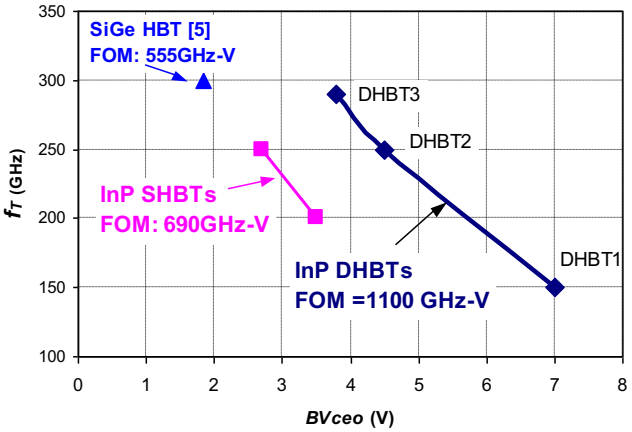


Figure 6. A comparison of f_T vs $BVceo$ for InP DHBTs, InP SHBTs and SiGe HBT [5]. FOM, $f_T \bullet BVceo$, is shown in chart for each technology.

Table 1. Summary of typical DC and RF data for GCS' InP HBT devices. SHBT and DHBT1 are first-generation foundry devices. DHBT2 and DHBT3 are advanced high f_T devices.

HBT Parameters	Unit	SHBT	DHBT1	DHBT2	DHBT3
Emitter Size	μm^2	1x3	1x3	0.8x3[#]	
Beta at *Jc*=100kA/cm^2		35	35	40	40
Typical operating current density, *Jct*	kA/cm^2	100	100	200	200
Maximum operating current density, *Jcm*	kA/cm^2	200	200	300	300
Typical operating voltage, Vce	V	1.0	2.5	1.5	1.0
Base-collector breakdown voltage, *BVcbo*	V	4.0	9	5.5	4.5
Collector-emitter breakdown voltage, *BVceo*	V	3.5	7	4.5	3.8
Vce offset voltage, Vceoffset	V	0.15	0.15	0.15	0.15
f_T (at Max allowed operating current)	GHz	200	150	250	290
fmax (at Max allowed operating current)	GHz	200	150	240	250
Thermal resistance, Rth	^{o}C/mW	9.9	5.3	5.3	5.3

[#]: 0.8x5 and 0.8x10 μm^2 devices have the same DC (scaled) and RF performance as those of 0.8x3 μm^2 devices except for Rth.

Table 1 summarizes the DC and RF performance of all GCS InP HBT devices. SHBT and DHBT1 are first-generation devices for 40-50Gbps applications as described in a previous publication [1]. DHBT2 and DHBT3 are new technologies with ultra high f_T. The advantages of a DHBT structure are not only to achieve higher f_T and higher *BVceo* simultaneously but also to provide lower thermal resistance as compared to that of SHBT. In comparison with SiGe HBT technology, the performance parameters of InP DHBTs shown here are much better than those of SiGe HBTs. For example, a 300GHz-f_T SiGe HBT has a *BVceo* of only 1.85V and it requires much smaller emitter size and 10 times higher current density than its InP DHBT counterpart reported in this work in order to achieve the same 300GHz f_T [5].

Device Modeling

We have modeled all three different-size devices for both DHBT2 and DHBT3 using measurement data at different bias conditions (*Vce* from 1.0V to 2.0V and *Jc* from 30kA/cm^2 to 300kA/cm^2) and at three temperatures, (25, 50 and 75^{o}C). ADS design kits have been developed for this technology. An example of good fitting between modeled and measured data is shown in Fig. 3 for DC IV curves. Fig. 7 shows good fitting of s-parameter for a 0.8x5 μm^2 DHBT3 device at *Jc* of 200kA/cm^2 and *Vce* of 1.5V in the frequency range of 0.5 to 40GHz.

Reliability

We have also completed qualifications of DHBT2 and DHBT3 devices by high temperature stress test. HTOL test was performed at two different junction temperatures, 248 and 269^{o}C, at *Jc* =300kA/cm^2. Four groups with ten 0.8x3μm^2 devices in each group were tested. Fig. 8 shows the normalized beta versus high-temperature stress time at *Vce*=1.25V, *Jc*=300kA/cm^2 and *Tj*=248^{o}C for 10 DHBT3 devices. With the device failure criterion defined as 20% beta degradation at *Jc*=100kA/cm^2, the MTTF for this group

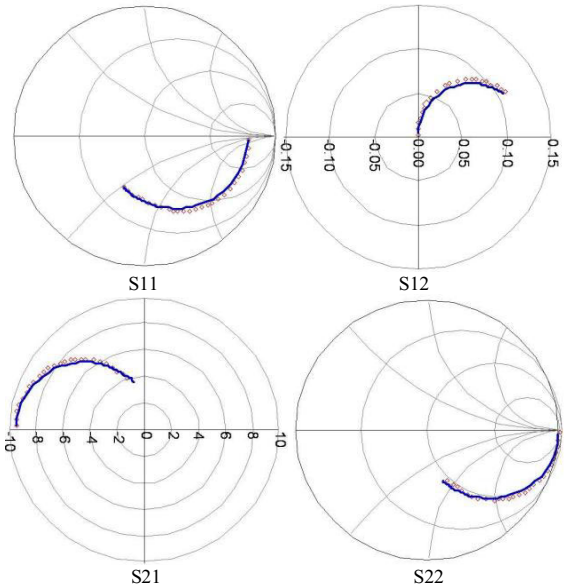


Figure 7. Measured (solid line) and modeled (dots) s-parameters for a 0.8x5 μm^2 DHBT3 device at *Jc*=200kA/cm^2 and *Vce*=1.5V in frequency range from 0.5 to 40GHz.

was 1028 hours. There were no infant failures in all groups tested. The typical device failure mode was base current increase. Fig. 9 shows the Gummel plots of a failed device before and after 1661 hours of high-temperature and high-current stress. The base current increased significantly in the low voltage region, mainly due to base surface recombination current increase, which is the typical HBT failure mechanism. Fig. 10 shows the Arrhenius plots for both DHBT2 and DHBT3 devices at two temperatures. The extrapolated MTTF is >2x10^6 hours at *Tj* =125^{o}C, and the activation energy (Ea) is >1.1eV, which could meet most application requirements. To the best of our knowledge, most InP HBT reliability data reported in the literature have been tested at *Jc* of about 100kA/cm^2 [6]. The reliability data of this work show that DHBT2 and DHBT3 have excellent reliability at *Jc* of 300kA/cm^2.

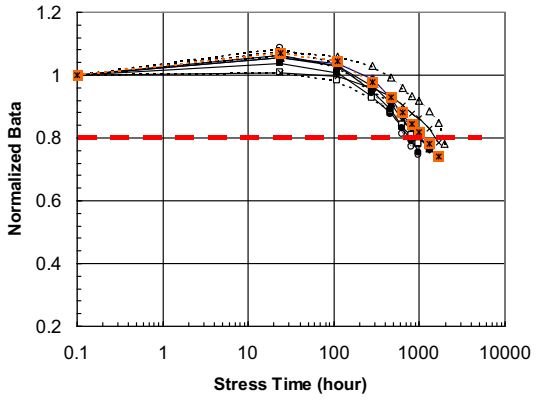


Figure 8. Normalized beta vs high temperature stress time of 10 DHBT3 devices at *Vce*=1.25V, *Jc*=300kA/cm^2 and *Tj*=248 °C.

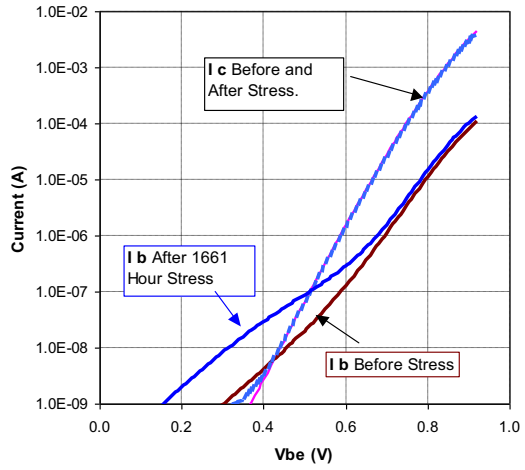


Figure 9. Gummel plots of a 0.8x5 μm^2 DHBT device before and after 1661 hour stress.

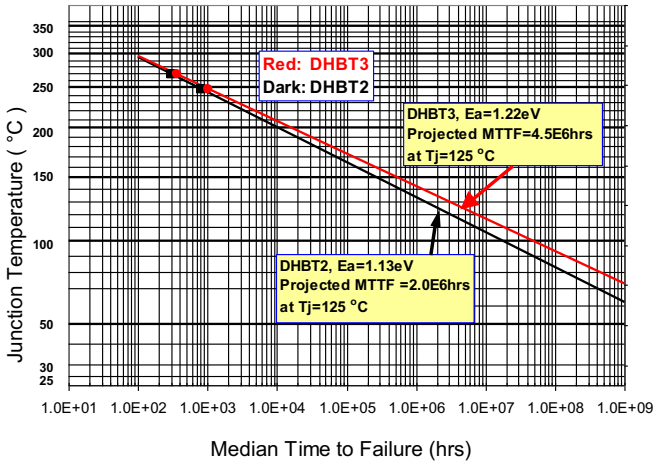


Figure 10. Arrhenius plots for both DHBT2 and DHBT3 at two temperatures. Extrapolated MTTF >2x10^6 hours at *Tj* = 125 °C and Ea >1.1eV.

CONCLUSIONS

In summary, we have developed and qualified an ultra-high-f_T InP/InGaAs DHBT technology for foundry service. Relationship between f_T and *BVceo* has been studied with different collector designs. Two DHBT devices with f_T-*BVceo* trade-offs are available in this technology. f_T of up to 300GHz and *fmax* > 250GHz for DHBT3 device with *BVceo* of 3.5V have been achieved. DHBT2, which has *BVceo* of 4.5V and f_T of 250GHz, is a good candidate for applications that require higher breakdown voltage. ADS design kits have been developed for this technology. Both DHBT2 and DHBT3 devices are very reliable with MTTF >2x10^6 hours at *Tj* of 125°C. This InP/InGaAs DHBT technology is an ideal candidate for 100Gbps electronic circuits such as TIA, and for high-speed digital, millimeter-wave, and mixed-signal circuits.

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ACRONYMS

HBT: Heterojunction Bipolar Transistor
DHBT: Double Heterojunction Bipolar Transistor
SHBT: Single Heterojunction Bipolar Transistor
f_T : Cutoff frequency
fmax: Maximum oscillation frequency
Jc: Collector current density
|H21|: Small signal current gain
MIM: Metal-Insulator-Metal
TFR: Thin Film Resistor
HTOL: High Temperature Operating Life
Tj: Junction temperature
MTTF: Median Time To Failure.
Ea: Activation energy
TIA: Transfer-Impedance Amplifier