Investigation and Improvement of Early MIM Capacitor Breakdown with a Focus on Edge Related Failures.

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Keywords: GaN HEMT, MMIC, MIM, capacitor, yield, quality

Abstract

When maintaining quality of a metal-insulator-metal capacitor process, it is important to fully understand the root cause for inferior breakdown of MIM PCM structures. This paper demonstrates a case of early capacitor breakdown and describes our method to identify defects before the destructive test with focus on edge-related failures. This led to understanding root cause and generating necessary experiments for improvement. A low-breakdown mode in the distribution was mostly eliminated through liftoff improvement and design rule adjustment.

INTRODUCTION

A high-voltage metal-insulator-metal capacitor (MIMCAP) process is necessary for any credible wide-bandgap MMIC process, but not at the expense of capacitor density. Cree's commercial wide-bandgap MMIC foundry process includes a metal-insulator-metal (MIM) capacitor with nominal 180 pF/mm^2 and >1E7 hour MTTF at 100 V and 125 °C. The high-voltage capacitor comprises a PECVD dielectric between an upper electrode (M2) and lower electrode (M1). Both electrodes consist of an evaporated Ti/Pt/Au film that is roughly 3 microns in thickness and defined with liftoff processing. In order to be a meaningful gauge of the production process, the active area of the "extrinsic" capacitor process-control monitor (C-PCM) is 0.1 mm^2.

The C-PCMs, processed alongside commercial MMICs, are electrically tested with a standard voltage ramp method as described by Yeats [1], using a high-voltage Keithley 237 SMA. Employing this method, the voltage is ramped in 0.5 V step increments from use voltage until catastrophic failure of the capacitor (V_{BD}), utilizing dwell times ranging from 25 ms to 100 ms and measuring approximately >100 on-wafer capacitors.

Figure 1 displays a typical normalized breakdown voltage distribution for C-PCM test structures measured at the beginning of this study. A bimodal pattern is present, and capacitors that fail before 80% of the max breakdown voltage are considered premature failures. This is not a well-defined cutoff point, but simply a good transition point between the two modes. Capacitors in the lower population cannot be modeled using field-acceleration factors derived from the median of the population, and application of the TDDB method for lifetime prediction would be questionable.

By testing each capacitor until failure, we can easily inspect them to roughly determine the failure location. Figure 2 displays the same data group as Figure 1, but separates the capacitors into center and edge fails. For the purpose of this study an "edge fail" is defined as a cap failure point that destructively alters both M1 and M2 edges. The percentage of edge fails versus center fails is much higher than it should be based on perimeter-to-area ratio, and the average failure voltage is much lower. This accounts for the majority of the low-voltage failures that are not in-family with the upper three quartiles of the distribution.

In an effort to understand the cause of these edge failures, a random sample of caps were inspected with a Scanning Electron Microscope (SEM) at various points throughout the fabrication process. After electrical testing, the capacitors were re-inspected to see if previously noted defects resulted in premature failures.

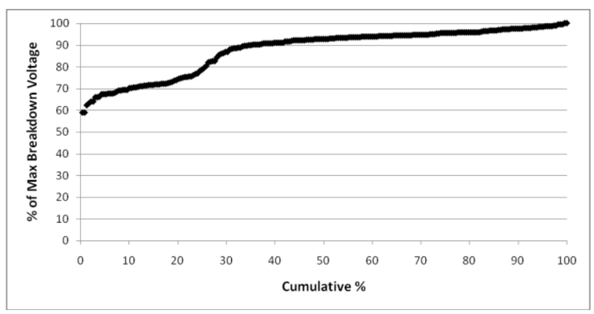

FIGURE 1: TYPCIAL BREAKDOWN DISTRIBUTION FOR EXTRINSIC CAPACITOR TEST STRUCTURES

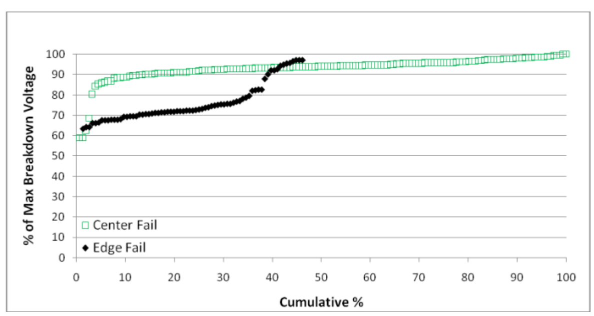

FIGURE 2: TYPICAL BREAKDOWN SEPERATED BY FAILURE MODE: CENTER (open) VS. EDGE (solid)

CRITICAL INSPECTION AND ROOT CAUSE ANALYSIS

Premature failures can be the result of substrate defects, particles, metal roughness or any number of possible processing issues [2]. Indeed, our inspections completed before the upper electrode formation showed these routine quality issues, but none of these inspections clearly indicated they were related to edge failures.

Detailed SEM inspections completed after M2 liftoff revealed defects similar to the one shown in Figure 3. Once liftoff was complete, some areas contained excess metal along the edge of the metal pad. As shown in the upper-right inset of Figure 3, this metal tag remains connected to the upper metal pad, but also extends out and over the edge of the lower pad. The lower-left inset exhibits that the edge defect can also be evident in an automatic optical inspection station.

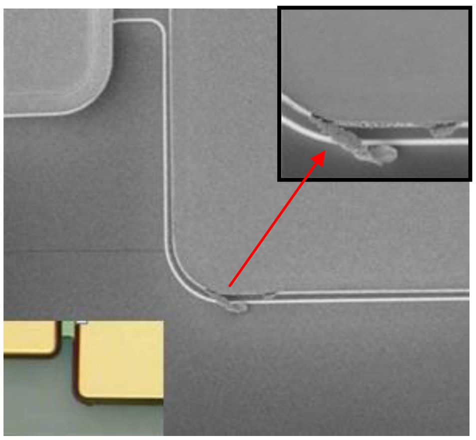

FIGURE 3: SEM IMAGE OF METAL LIFTOFF ISSUE NOTED AFTER M2 LIFTOFF AND BEFORE ELECTRICAL TESTING

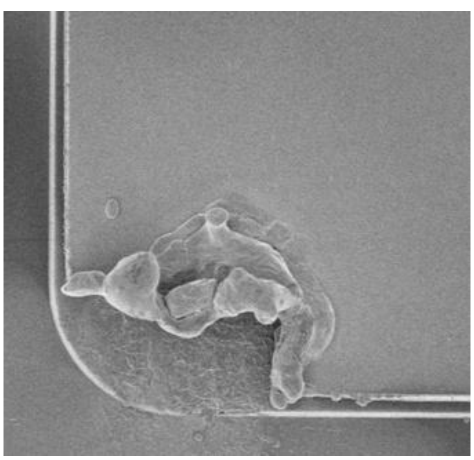

FIGURE 4: SEM IMAGE OF CAPACITOR SHOWN IN FIGURE 3 POST ELECTRICAL TEST

After electrical testing, re-inspection of the same sites showed failures at the exact locations of the metal liftoff issue. This particular capacitor in Figure 3 failed at 74% of the maximum breakdown voltage, putting it in the low failure category and confirming M2 liftoff tags as a capacitor reliability concern and yield detractor.

Samples having a known liftoff issue were introduced to a short Au etch and then fresh C-PCMs were tested to see if the etch back or removal of these metal tags would improve the capacitor electrical performance. Results shown in Figure 5 indeed show a significant improvement in capacitor breakdown. A large portion of the lower voltage breakdown failures were eliminated, thus supporting the idea that poor metal liftoff was a significant contributor to the lower voltage failures.

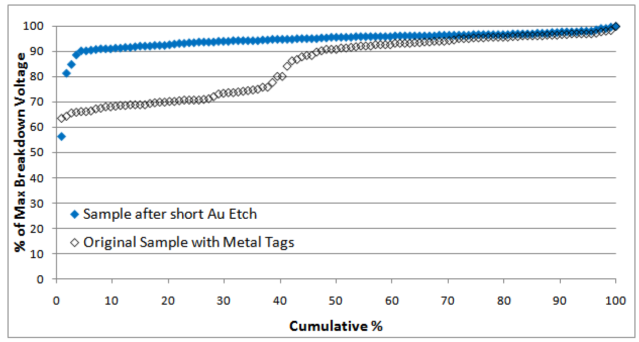

FIGURE 5: AU ETCH BACK BREAKDOWN VOLTAGE IMPROVEMENTS.

IMPROVEMENTS

Understanding the root cause for early edge capacitor failures led the way for a few small process adjustments to improve liftoff quality. At the same time the distance between the electrode edges was doubled to understand if that would mitigate the risk of occasional liftoff problems becoming pathways for early capacitor failure.

Since the M2 liftoff quality needed to be addressed, an experimental focus was placed on optimizing the photoresist profile. Based on process experience, tests were performed to evaluate photoresist pattern development in order to generate a more robust resist sidewall profile. The experiment resulted in changing the developer agitation mode and develop time, translating to a larger overhang and slightly more negative slope of the liftoff resist.

In addition to the process changes discussed above, we also observed that the base focus position of the stepper had a distinct influence on the shape of the sidewall profile. By adjusting the base focus off the optimum resolution position, we found that the profile could be tailored to a more optimum shape for metal liftoff. Through further experimentation, we determined the ideal focus process window resulting in cleaner metal liftoff processing and thus a reduction in low breakdown cap failures.

Figure 6 shows the results of the changes discussed above. Each change, liftoff improvements and an increase in edge spacing, results in far less early failures. Combining the two changes provides even further improvement, which indicates a potential for further liftoff process optimization.

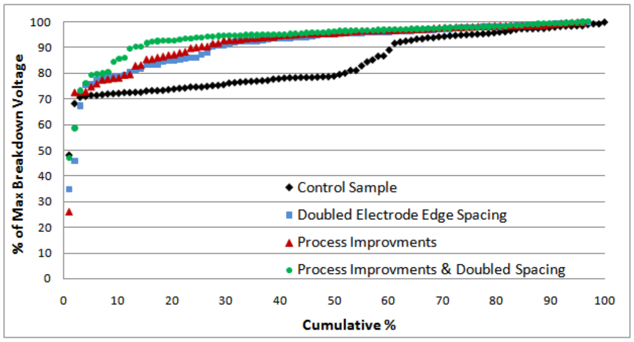

FIGURE 6: BREAKDOWN DISTRIBUTIONS FOR PROCESS IMPROVEMENTS AND LAYOUT CHANGE.

SUMMARY

For a commercial wide-bandgap MMIC foundry process, it is important to understand root cause of lower-than-expected breakdown on MIM PCM structures. This paper describes a case of early capacitor breakdown attributable to capacitor edge-related defects. In contrast to usual post-failure analysis techniques, inspection of defects prior to destructive test led to discovery of root cause and allowed for minor process adjustments, improving M2 liftoff and reducing edge failure frequencies. Minimizing these failure mechanisms allows for increased quality and reliability of capacitors used in high-power GaN MMICs.

REFERENCES

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[2] J. Cotronakis, "Continuous Defectivity Improvements and Impact on High Density Metal-Insulator-Metal (HDMIM) Capacitor Yields," 2004 International Conference on Compound Semiconductor Manufacturing Technology.