High efficiency and low leakage AlGaN/GaN HEMTs for a robust, reproducible and reliable X-band MMIC space technology

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Abstract

We report on epitaxial growth, processing, device performance and reliability of our GaN HEMT and MMIC technology on 3-inch SiC substrates. Processing is performed in MSL technology consisting of frontside processing (0.25 µm gate length and complete passive matching network), substrate thinning to 100 µm, and backside processing including front-to-back substrate via holes. The process technology exhibits excellent uniformity across a single wafer as well as high reproducibility from wafer to wafer. HEMTs have high PAE (50% without intentional harmonic matching) and low leakage currents (below 100 µA/mm at a drain bias as high as 150 V). We have fabricated one-stage and two-stage MMICs with efficiencies beyond 40%. The reliability of our MMIC technology is investigated using one-stage MMICs under RF operation at 30 V showing a drift of around 0.3 dB in output power over 1000 h of operation at a Raman calibrated channel temperature of 185°C.

INTRODUCTION

Due to its wide band gap, high breakdown field, current density and saturated velocity, group III nitrides are well suited for high temperature and high power applications from RF to millimeter wave frequencies. A very attractive application of GaN HEMTs are high-power, high-efficiency GaN MMICs at X-Band frequencies for radar, communication and space applications [1].

Here we report on epitaxial growth, processing technology, device performance and reliability of our 3-inch GaN HEMT and MMIC technology. Finally, we present initial results from space assessment tests.

EPITAXIAL GROWTH

Incoming 3-inch 4H-SiC(0001) substrate wafers are first classified using polarized light imaging in order to examine the defect distribution. The AlGaN/GaN heterostructures are then grown in a modified 12×3-inch Aixtron MOCVD reactor. Epitaxial growth starts with an AlN nucleation layer followed by a GaN buffer layer and the AlGaN barrier. The structure is capped with a thin GaN layer. Both the composition and the thickness of the active region are calibrated by high resolution x-ray diffraction (HRXRD) in conjunction with dynamical simulation of the profiles.

For a 22 nm $Al_{0.22}Ga_{0.78}N$ barrier and a 3 nm thin GaN cap typical sheet carrier concentrations and mobilities are 8×10^{12} cm^{-2} and 1500 cm^2/Vs yielding sheet resistances around 500 Ω/sq that are reproducibly obtained with a uniformity better than 2% across the entire wafer. The threading dislocation density is in the low 10^8 cm^{-2} range as determined by plan-view transmission electron microscopy, the surface roughness as studied by atomic force microscopy (see Figure 1) is well below 0.5 nm over an area of 10×10 μm^2, the buffer isolation resistance at 60 V is well above 10^{12} Ω/sq for a 4 µm gap test structure.

Processing is performed in microstrip line technology consisting of frontside processing, substrate thinning to 100 µm and backside processing including front-to-back substrate via holes, see [2]. Our HEMTs and MMICs feature 0.25 µm gate length HEMTs in combination with thin film NiCr resistors, high-voltage MIM capacitors and inductors for impedance matching to a 50 Ω environment, see Figure 2 for a chip photograph. Device fabrication is performed using standard processing techniques involving electron-beam and optical lithography: stepper alignment for frontside and contact mask alignment for backside device definition. Device processing is designed for homogeneity and

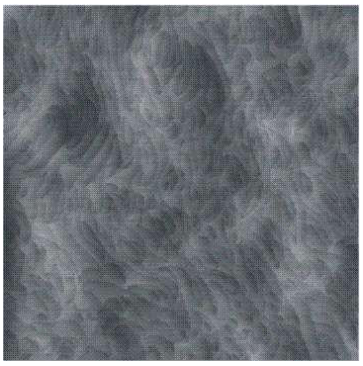

Figure 1: Typical atomic force micrograph (10×10 μm^2 area) of an AlGaN/GaN structure grown for this sample series. The root mean square surface roughness is 0.25 nm.

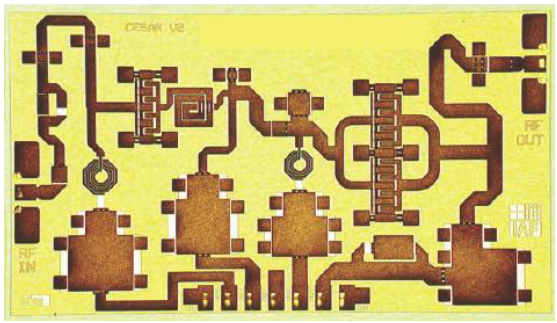

Figure 2: Chip photograph of a fully processed two-stage MMIC in microstrip line technology.

reproducibility.

FRONTSIDE PROCESSING AND HEMT PROPERTIES

We employ a Ti/Al/Ni/Au based metal stack in combination with an RTA step (825°C, 30 s) in order to achieve an ohmic contact with low contact resistance (< 0.3 Ω×mm) as well as smooth edges for well defined e-beam marker detection. The gate process consists of two steps: First a window is etched into the passivation (typically 100 nm SiN) in order to define the Schottky area and then the actual gate metal (Ni/Au) is deposited where the overhang towards source and drain defines the integrated gate-terminated field plate. In a second step an optional source terminated field plate is applied after passivation of the gate metal.

After processing we first investigate the electrical properties of the devices. Of prime interest are efficiencies and leakage currents in order to minimize the required prime power, to keep self-heating at a low level for acceptable channel temperatures during operation and to finally obtain decent reliability. HEMTs have both high PAE and low leakage currents, thus demonstrating that we have

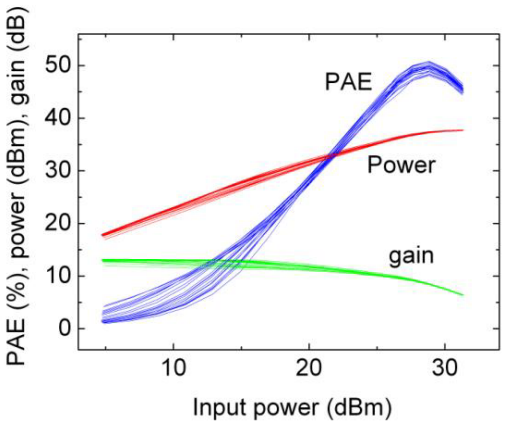

Figure 3: 10 GHz loadpull mapping overlay at 30 V of 0.25 µm gate length HEMTs with 1 mm gate periphery across all 21 cells of an entire 3-inch wafer.

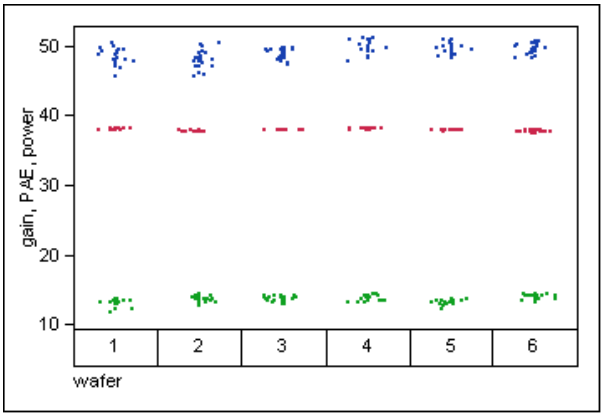

Figure 4: PAE (blue, top), output power (red, middle) and linear gain (green, bottom) of a 1 mm gate width HEMT for a batch of 6 wafers as determined from 10 GHz loadpull mapping. Note the excellent reproducibility and homogeneity.

successfully achieved high isolation and low trap densities with the intrinsic transistor. In Figure 3 we show results from 10 GHz continuous-wave loadpull mapping at 30 V drain bias of a 1 mm gate width HEMT structure without intentional harmonic matching across an entire 3-inch wafer. All 21 cells are measured using the same tuning settings in order to fully investigate the uniformity of epitaxial growth and device processing. The mean values for PAE, output power and linear gain are 50%, 38 dBm (6 W/mm) and 13 dB with a scatter around 2%. In Figure 4 we show a summary of these measurements for a batch of 6 wafers. For all wafers we observe very similar data in PAE, power and gain indicating the uniformity and reproducibility of epitaxial growth and processing technology.

For the same set of wafers we investigate the pinch-off of HEMTs. In Figure 5 the drain leakage current density at 150 V drain bias and -7 V gate bias, i.e. well below the

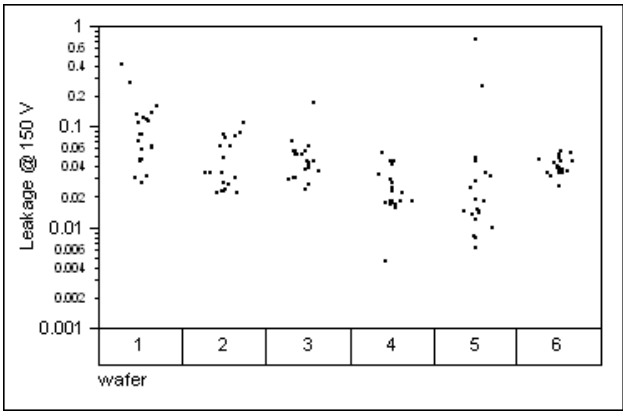

Figure 5: Leakage currents (mA/mm) of a process control monitor structure at a drain bias of 150 V and a gate bias of -7 V for a batch of 6 wafers.

threshold voltage of -2.5 V. For all wafers the leakage currents are around or below 100 µA/mm demonstrating excellent pinch-off even at such large drain voltages.

PASSIVES, BACKSIDE PROCESSING AND MMIC PROPERTIES

The passive MMIC matching network consists of MIM capacitors, inductors and thin film resistors. As a metric for homogeneity we utilize the small signal gain of the two stage MMIC shown in Figure 2 which features all passive components. The overlay of the frequency dependent small signal parameters of all 21 cells is shown in Figure 6. We have achieved good uniformity across the entire wafer demonstrating the uniformity of our processing technology. This result is in good agreement with the uniformity and reproducibility of the individual passive elements.

For an MSL process it is necessary to reproducibly achieve substrate front to back via holes with a low resistance. In Figure 7 we show the resistance of a test structure for all wafers in a batch. The structure consists of two via holes. The resistance is reproducibly and uniformly below 5 mΩ per individual via hole for all wafers in the batch. This result demonstrates the uniformity and reproducibility achieved in our via hole fabrication consisting of mask definition, etching and metallization.

The entire backside processing furthermore includes mounting on a carrier wafer and mechanical thinning down to the desired thickness of 100 µm. The mechanical and thermal stress during thinning and etching needs to be reduced to a level where transistor performance does not change (thermal effects during the actual measurement excluded). In our experience a suitable combination of frontside processing, carrier material, adhesive for mounting, thinning conditions and etching conditions are required in order to achieve this goal. The change in leakage current from a wafer after frontside processing to the same wafer after backside processing is, if any, negligible, see Figure 8. Similarly, other parameters such as threshold voltage, transconductance and DC-to-RF dispersion do not change.

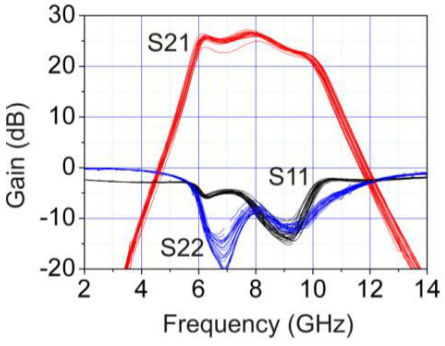

Figure 6: Small signal mapping overlay of all 21 cells across a 3-inch wafer of a two-stage MMIC at 30 V drain bias. Note the good homogeneity.

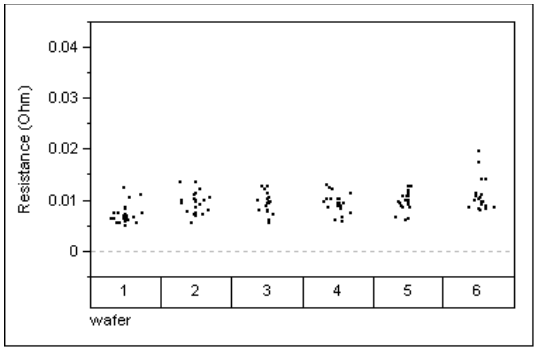

Figure 7: Resistance of a test structure consisting of two front to back substrate via holes.

We have fabricated one-stage and two-stage MMICs using the X-band technology presented here. One-stage amplifiers are mainly utilized for process control monitor purposes and reliability, see below. Using suitable harmonic termination techniques on-wafer we have realized one-stage MMICs with more than 55% PAE at 10 GHz [3] in agreement with the PAE on HEMT level reported above without harmonic termination. The large signal properties of our small gate width two-stage MMICs under continuous wave conditions at 30 V drain voltage are characterized by a PAE above 40%, a gain around 20 dB and an output power close to 5 W/mm at a frequency of 8 GHz. Narrowband HPAs achieve a maximum output power and PAE of 20 W and 40%, respectively, at 9 GHz. Broadband amplifiers reach a output powers around 20 W with >30 % PAE between 9 and 11 GHz. [4].

RELIABILITY

The reliability of our MMIC technology is investigated using one-stage MMICs having a gate width of 1 mm which are measured in an RF package. The overall reliability is

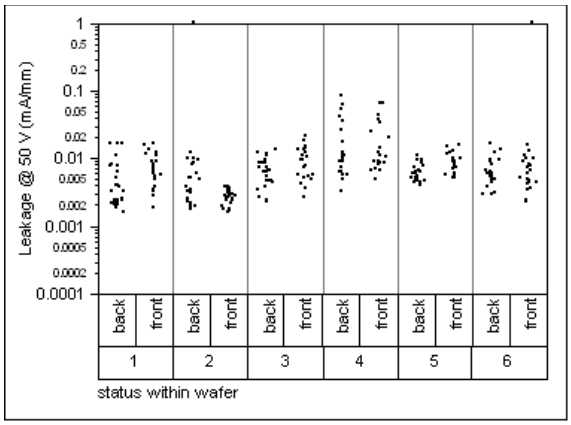

Figure 8: Leakage current of process control monitor structure after frontside processing ("front") and after backside processing ("back") for 6 wafers in a batch.

very promising. Figure 9(a) shows results from an RF test carried out at 10 GHz with a supply voltage of 30 V. The channel temperature is around 185°C as determined by Raman thermography [5]. The gain of our devices changes by only up to 0.3 dB within 1000 h. During the test we also measure gate and drain currents, see Figure 9(b). The drain current changes by less than 5% whereas the gate currents remain below 50 µA/mm throughout the test.

INITIAL SPACE ASSESSMENT TESTS

The polar surface of GaN makes this material ideal for gas sensors based on the shift of the surface potential due to adsorbed gas species. However, for space applications it is necessary to reduce the sensitivity to hydrogen (as present in a space environment) as much as possible in order to allow stable operation. In order to test our technology PCM structures were packaged and exposed to 5% hydrogen / 95% nitrogen ambient at 250°C for 24 h. Control samples were stored in 100% nitrogen under otherwise identical conditions. Electrical parameters were measured before storage and after exposure. For our samples the change in threshold voltage, transconductance and leakage is well below 10% for both ambients indicating also promising space capabilities of our devices.

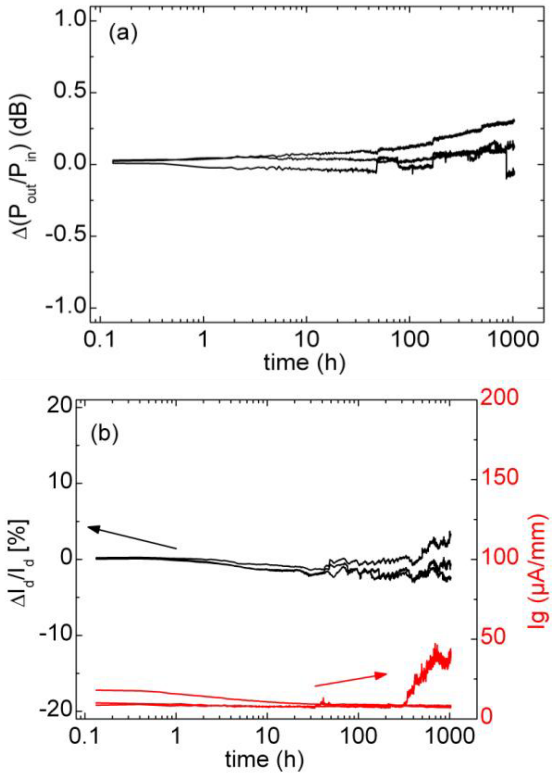

Figure 9: Reliability investigation (10 GHz, 30 V) of a one-stage MMIC at a channel temperature of about 185°C: (a) change in gain, (b) change in drain currents (top) and evolution of gate currents (bottom).

CONCLUSIONS

We have fabricated AlGaN/GaN HEMTs and MMICs in microstrip line technology on 3-inch SiC substrates. The overall performance of our HEMT devices exhibits excellent homogeneity and reproducibility with PAE around 50% operated at 30 V under 10 GHz continuous-wave operation. The leakage currents are as low as 100 µA/mm at 150 V drain bias. One- and two-stage MMICs reach PAE above 40%. The reliability investigations of our MMIC technology under 10 GHz continuous wave operation at 30 V return a drift around 0.3 dB in output power over 1000 h of operation at a Raman calibrated channel temperature of 185°C.

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ACRONYMS

MSL: Microstrip Line Technology
HEMT: High Electron Mobility Transistor
MMIC: Monolithic Microwave Integrated Circuits
PAE: Power Added Efficiency
MOCVD: Metal Organic Chemical Vapor Deposition
MIM: Metal Insulator Metal
RTA: Rapid Thermal Annealing
PCM: Process Control Monitor