

Stable and reproducible AlGaIn/GaN-HFET processing highly tolerant for epitaxial quality variations

P. Kurpas, I. Selvanathan, M. Schulz, H. Sahin*, P. Ivo, M. Matalla, J. Splettstoesser*, A. Barnes**, J. Würfl

Ferdinand-Braun-Institut für Höchstfrequenztechnik (FBH), Gustav-Kirchhoff -Str. 4, 12489 Berlin, Germany

Phone: +49-30-6392-2674, fax: +49-30-6392-2685, e-mail: paul.kurpas@fbh-berlin.de

*United Monolithic Semiconductors GmbH, Wilhelm-Runge-Str. 11, 89081 Ulm, Germany

** ESA/ESTEC, Keplerlaan 1 P.O. Box 299, 2200 AG Noordwijk ZH, The Netherlands

Keywords: AlGaIn/GaN HFET, HEMT, processing reproducibility issues, gate technology, benchmarking epitaxy

Abstract

AlGaIn/GaN HFETs have been fabricated on epitaxial wafers, using nominally an identical epitaxy procurement specification, procured from 9 different vendors worldwide. A stable and reproducible device processing technology was established in order to allow the performance attributes of the epitaxial wafers to be benchmarked. In order to obtain a fair vendor comparison, the processing modules were modified such that processing could be relaxed to allow fabrication on wafers with varying quality. On the example of the effect of wafer warp it is shown that especially gate technology has had to be adapted: non-optimized gate profiles lead to higher leakage currents and worse reliability performance. Results from on-wafer test structures and device performances verified differences in material qualities and allowed for reliable vendor benchmarking.

INTRODUCTION

AlGaIn/GaN HFET transistors on SiC substrates are enabling devices for highly efficient RF power devices. Remarkable progress was achieved in the last years regarding the epitaxial material supply chain as well as device fabrication. Especially, the challenge for robust and reliable devices shows impressive improvements [1].

FBH has been selected by the European Space Agency (ESA) to perform a challenging research project on benchmarking epitaxial qualities of GaN-HEMT wafers [2]. The project goal was to compare the technology levels achieved in Europe with the worldwide status in this field. For this purpose FBH acquired wafers with a defined epi-structure from 9 vendors in Europe, in the US and in Japan.

As the first step, extensive non-destructive material characterizations were done on each wafer [2]. Thus, first comparison of wafer qualities was obtained by this way.

However, a real meaningful qualification of an epi-wafer can only be obtained from manufacturing active devices and performing small signal and large signal testing under representative operating conditions. To allow a true and proper comparison of device performance that can be related back to material properties, a stable and reproducible fabrication process is an indispensable requirement. Furthermore, the processing should be as invariant as possible toward the observed differences in wafer qualities.

In this paper we describe some key issues solved during the project work. The successful achievement of the benchmarking goals is confirmed by device results.

EXPERIMENTAL

A special requirement for processing, that is compatible with the benchmarking task, is how best to cope with different wafer qualities. One important property of a GaN-HEMT wafer is its bow. Figs. 1 and 2 show two extreme examples of warped wafers within the benchmarking wafer group. Strongly bowed wafers make the lithography difficult reducing the device yield.

Therefore, at FBH proper reconfiguration of the vacuum chuck in the optical i-line stepper was done in order to improve the flattening of warped wafers under vacuum condition. Fig. 3 visualizes the possible reduction of wafer bow. As expected, the warp reduction is much more effective in the case of convex bowed wafers.

Taking account of these bow changes on vacuum chucks during wafer handling was thus important for both optical but especially for electron beam lithography. Careful focussing optimization for the optical stepper and proper positioning of alignment marks in the case of e-beam writing is of particular importance. This approach allowed FBH to

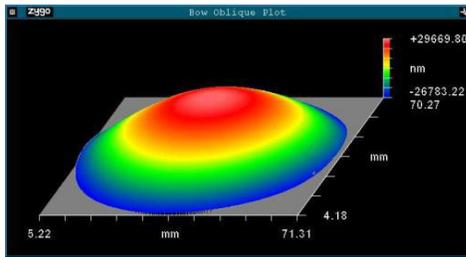


Fig. 1: Example for convex bowed wafer with very large total warp of 60 μm .

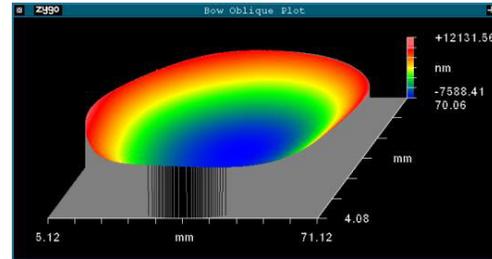


Fig. 2: Example for concave bowed wafer with total warp of 18 μm .

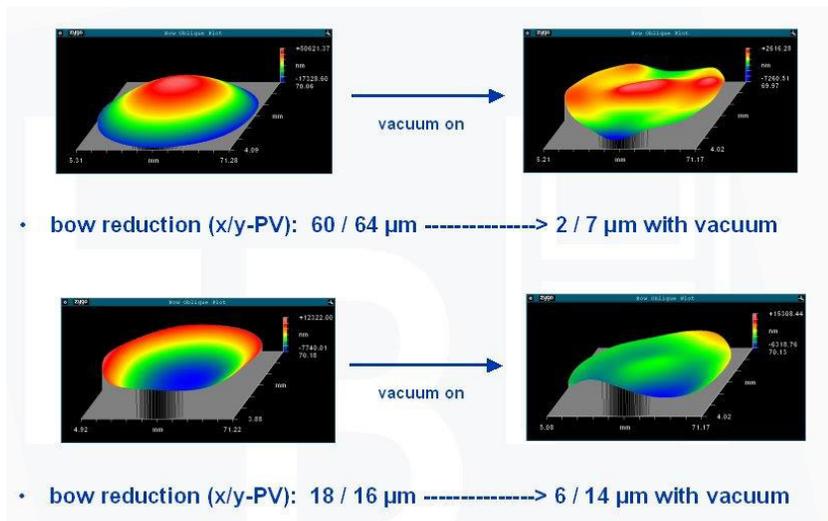


Fig. 3: Effect of vacuum chuck on convex or concave bowed AlGaIn/GaN-HFET-wafers.

successfully process wafers with high device yields in the 90 % region regardless of the initial wafer warp values encountered which were typically in the range 3 μm - 30 μm .

In addition the device processing should not affect the intrinsic device performance, since ultimately this is primarily defined by the epitaxial layer quality. Thus, a "conventional" T-type gate module was chosen in order to minimize the processing impact on the epitaxial material which could occur if other, more yield sensitive, approaches for gate formation are used, for instance due to the required etching of foot trenches. Fig. 4 confirms that perfect fabrication of 250 nm long T-gates was achieved.

However, the bowed and/or irregular shape of the wafers still makes the uniform e-beam gate lithography difficult. Fig. 5 shows a possible gate non-perfection observed on test wafers at a few "stitched" e-beam writing areas of a dice. At a distance of ~ 100 nm the gate foot resist was not completely opened. By direct comparison of the same type of transistors, with and without such a "stitching-fault", we have seen that this non-perfectness leads to a three times

higher current at pinched-off condition (figs 6a and 6b). Furthermore, the transistor's reliability is affected too, as verified by comparison of voltage step-stress measurements (fig. 7). After further optimization of the e-beam gate writing procedure, the "stitching-faults" could be fixed even on strongly bowed wafers leading to an optimized high yield process that was suitable for the benchmarking exercise.

DEVICE RESULTS

The established processing allowed stable and reproducible GaN-HEMT wafer fabrication. The first evaluation of material qualities was based on results from on-wafer test structures. Fig. 8 gives the results for sheet resistance mapped on pairs of wafers where first and second wafer were processed in two subsequent process runs, respectively. The variation of absolute values can be explained partially by variations in thickness and/or composition of the AlGaIn barrier layer, however the remaining differences give information on different channel properties. Furthermore, large differences in wafer uniformity between vendors can be concluded, too.

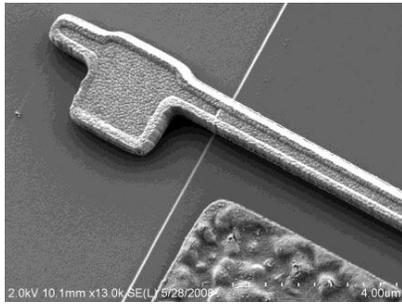


Fig. 4: SEM viewgraph of a T-gate with 250 nm gate length.

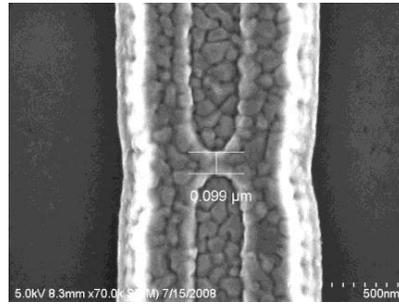


Fig. 5: SEM viewgraph of a "stitching-fault" in T-gate's profile.

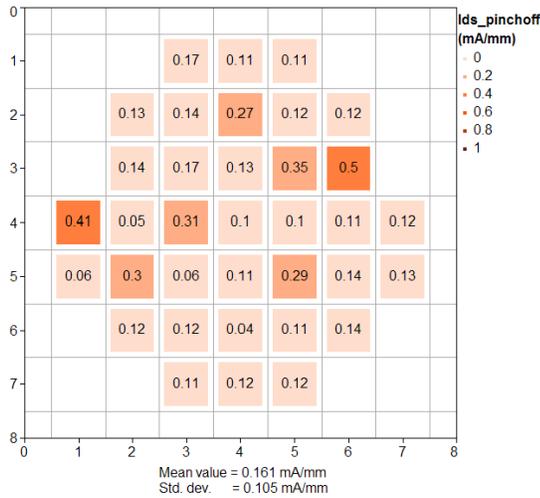


Fig. 6a: Rest current at pinched-off condition measured on transistors with perfect gate profile (2x125 μm).

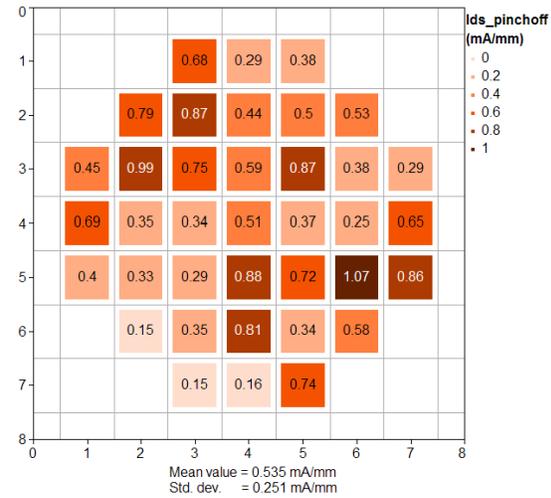


Fig. 6b: Rest current at pinched-off condition measured on transistors affected by gate "stitching-fault" (2x125 μm, neighbour transistor on the same wafer as shown in fig. 6a).

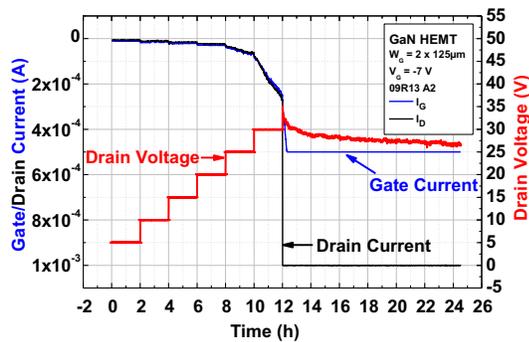


Fig. 7a: Voltage step-stress measurement on transistor with perfect gate profile.

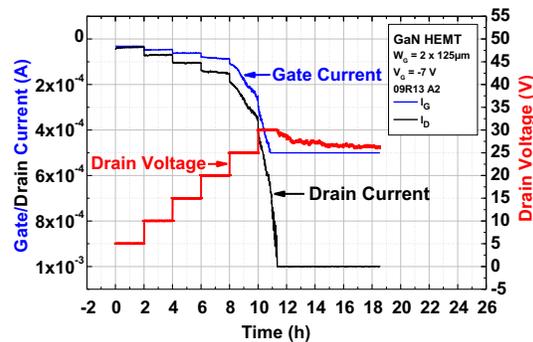


Fig. 7b: Voltage step-stress measurement on a transistor affected by gate "stitching-fault".

Fig. 9 shows typical measured dc transconductance as an example for transistor related properties. It is clearly visible that the obtained transconductances differs in a large region between the vendors despite of their "nominally the same" layer structures.

The processing reproducibility is confirmed by the finding that the absolute value and again the wafer uniformity were reproduced for each particular vendor. For some vendors, however, the limited epitaxial run-to-run reproducibility is verified (e.g. vendors 2 and 3 in fig. 9). Thus, the information on particular epi-material quality is clearly determined and reproduced.

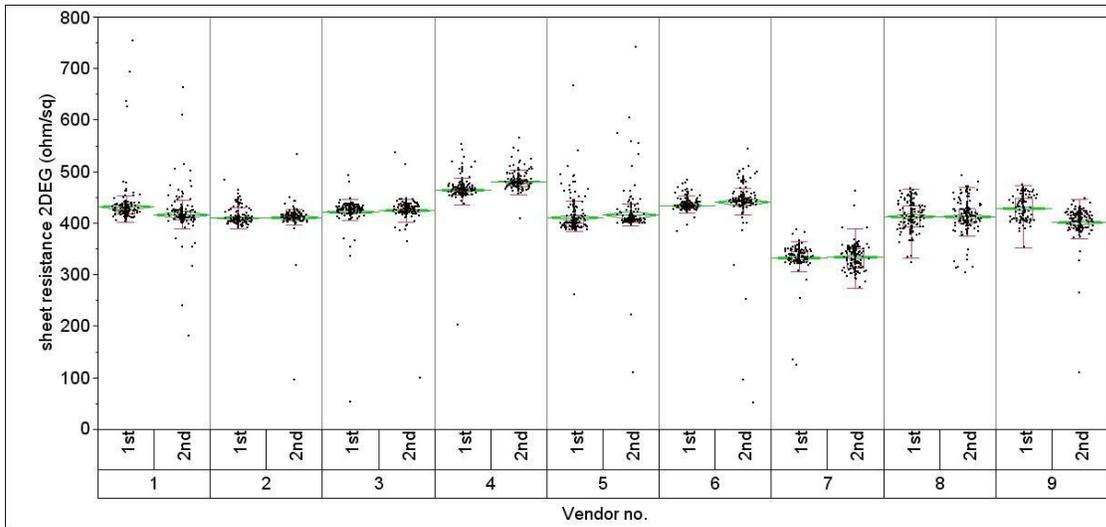


Fig. 8: Sheet resistance measured on pairs of wafers (1st and 2nd wafer) from 9 different vendors (vendors 1...9) processed in two subsequent runs (mappings of 148 TLM test structures each per 75 mm wafer).

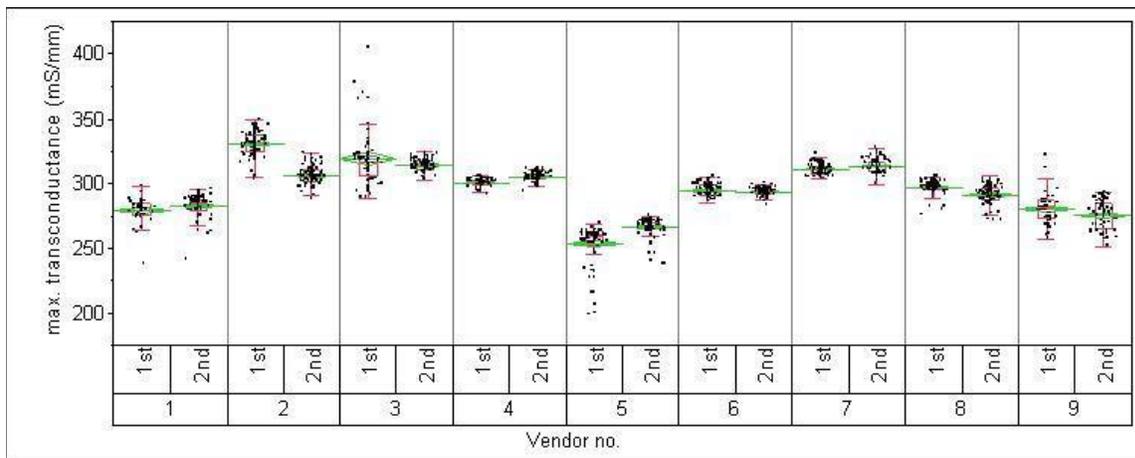


Fig. 9: Maximum transconductance of $2 \times 50 \mu\text{m}$ AlGaIn/GaN-HFET measured on pairs of wafers (1st and 2nd wafer) from 9 different vendors (vendors 1...9) processed in two subsequent runs (mappings of 148 transistors each per wafer). The order of vendors is changed here as compared with fig. 8.

CONCLUSIONS

Taking advantage of optimized technology the goal of the benchmarking project was successfully achieved. Based on reliable material and device results a fair "ranking" of epitaxial GaN-HEMT wafer vendors was obtained. The collected data provide a baseline technology reference for future space-approved GaN HEMT devices.

ACKNOWLEDGEMENTS

The authors would like to thank the process technology department at FBH for their expert technical assistance during wafer processing, and M. Mai, L. Schellhase and Y. Cankatan for their help on

measurements and data evaluation. Financial support by European Space Agency ESA/ESTEC under TRP contract 20328/06/NL/IA is gratefully acknowledged.

REFERENCES

- [1] M. Rosker, Ch. Bozada, H. Dietrich, A. Hung, D. Via, S. Binari, E. Vivierios, E. Cohen, J. Hodiak, 2009 CS MANTECH Technical Digest, pp. 7-10
- [2] "Performance Benchmarking of European GaN Epitaxial Wafer Suppliers", ESTEC/Contract No. 20328/06/NL/IA.
- [3] P. Kurpas, J. Würfl, A. Barnes, " Status of AlGaIn/GaN HEMT epitaxial wafer benchmarking", SPACE AGENCY-MOD WORKSHOP ON GaN MICROWAVE COMPONENT TECHNOLOGIES, Ulm, Germany, 30th – 31st March 2009