Enhancement-mode AlGaN/GaN HEMTs Fabricated by Standard Fluorine Ion Implantation

Hongwei Chen, Maojun Wang, Kevin J. Chen
Dept. of Electronic and Computer Engineering, Hong Kong University of Science and Technology, Hong Kong
Tel: (852) 2358-8530, Fax: (852) 2358-1485, Email: chwust@ust.hk

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Abstract: This paper presents a fabrication technology of enhancement-mode AlGaN/GaN HEMTs using standard fluorine ion implantation. An 80 nm silicon nitride layer was deposited on the AlGaN as an energy-absorbing layer that slows down the high energy (~25 keV) fluorine ions so that majority of the fluorine ions are incorporated in the AlGaN barrier. The threshold voltage was successfully shifted from -1.9 V to +0.6 V, converting depletion mode HEMTs to enhancement-mode ones. The fluorine ion distribution profile was measured by Secondary Ion Mass Spectrometry (SIMS) and is consistent with results from SRIM (The Stopping and Range of Ions in Matter) simulation.

Introduction:

Owing to superior physical properties such as high electron saturation velocity and high electric breakdown field, GaN-based high electron mobility transistors (HEMTs) are capable of delivering superior performance in microwave amplifiers, high power switches, and high temperature integrated circuits (ICs). Compared to the conventional D-mode HEMTs with negative threshold voltages, enhancement-mode (E-mode) or normally-off HEMTs are desirable in these applications, for reduced circuit design complexity and fail-safe operation. Several approaches have been developed to fabricate enhancement-mode AlGaN/GaN HEMTs, including recessed-gate [1, 2], fluoride plasma treatment [3-5], and p-type AlGaN cap [6] or InGaN cap [7]. Fluorine plasma treatment is a robust process that enables the channel threshold voltage modulation self-aligned to the gate electrode. However, there is no standard equipment for this process and various groups have reported a wide range of process parameters [3, 7-9].

In this paper, we demonstrate a fabrication process of enhancement-mode AlGaN/GaN HEMTs using standard ion implantation equipment. Ion implantation is widely used in semiconductor device fabrication with well-controlled dose and precise doping profile.

Device structure and fabrication:

The sample used in this work was a commercially available $Al_{0.26}Ga_{0.74}N$/GaN HEMT wafer grown by MOCVD on 4-inch silicon substrate. The capacitance-voltage (C-V) measurement by mercury probe yields an initial threshold voltage of -2.1 V for this sample.

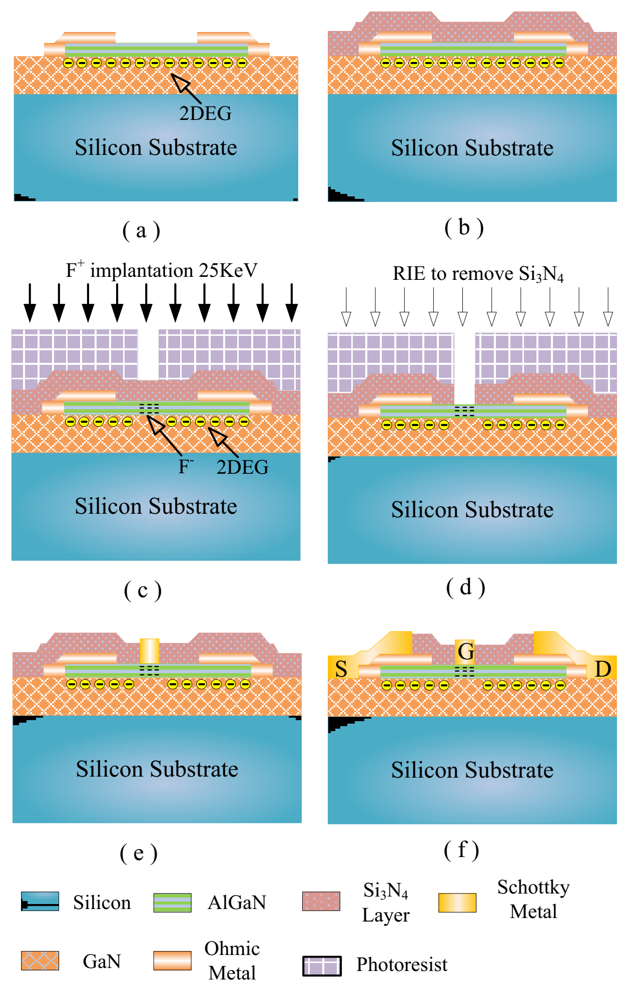

Fig. 1 Schematics showing the process flow of ion implanted E-mode HEMTs: (a) Active region and ohmic metal; (b) Si_3N_4 layer deposition; (c) Gate area definition and fluorine ion implantation; (d) Si_3N_4 layer etching; (e) Self-aligned gate metal deposition and lift-off; (f) Interconnection metal formation.

The process flow is illustrated in Fig. 1. At first, device mesa is formed using Cl_2/He plasma dry etching in an inductively coupled plasma reactive ion etching (ICP-RIE) system followed by the source/drain ohmic metal formation with Ti/Al/Ni/Au (20 nm/150 nm/50 nm/80 nm) annealed at 830 ˚C for 40s, as shown in Fig. 1(a). Then, a Si_3N_4 layer (~ 80 nm) is deposited on the sample by plasma enhanced chemical vapor deposition (PECVD) [Fig. 1 (b)]. After gate windows defined by photolithography, $^{19}F^+$ ions with an energy of 25 keV at a dose of 5.0×10^{12} cm^{-2} were implanted by Varian CF3000 ion implanter [Fig. 1 (c)], followed by low-power (50 W) CF_4 RIE etching to remove the Si_3N_4 layer [Fig. 1 (d)]. It should be noted that the ion energy of 25 keV is a value that can be stably obtained in standard ion implantation equipment, but will lead to F's penetrating deep into the GaN channel and buffer region. The Si_3N_4 layer was used as an energy-absorbing (or buffer) layer that slows down the F ions when they reach the AlGaN layer.

The gate electrode was then formed by E-beam evaporation of Ni/Au (~20 nm/280 nm) and lift-off [Fig. 1 (e)]. Finally, the interconnection metal is deposited and the silicon nitride over the active region was kept as the passivation layer [Fig. 1 (f)]. At last, the whole sample is annealed at 400 ˚C for 10 min to repair the implantation-induced damage in the AlGaN barrier and channel. The gate-source and gate-drain spacings are 1 µm and 2 µm, respectively. The E-mode HEMTs are designed with gate width of 10 µm for dc testing and 100 µm for RF characterizations. The D-mode HEMTs fabricated with the same process but without fluorine ion implantation are fabricated on the same sample as reference for comparison.

Device characteristics:

The transfer characteristics of E-mode HEMTs and D-mode HEMTs are plotted in Fig. 2. The over-etching of Si_3N_4 by the low-power CF_4 RIE shifts the threshold voltage of the D-mode HEMTs by about 0.2 V, from -2.1V to -1.9V. Comparing the transfer curves of E-mode and D-mode HEMTs, it can be seen that the threshold voltage is shifted from -1.9 V to +0.6 V by the fluorine ion implantation.

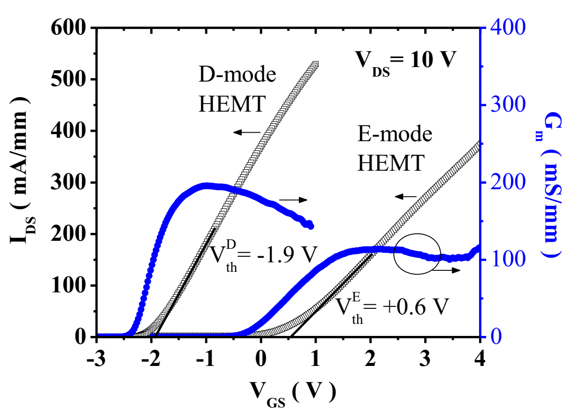

Fig. 2 Transfer characteristics of D-mode HEMTs and E-mode HEMTs with a gate length of 1 µm.

The peak transconductance G_m is about 200 mS/mm and 115 mS/mm for the D-mode HEMTs and the E-mode HEMTs, respectively. The smaller transconductance of the E-mode HEMTs is mainly due to the channel electron mobility degradation induced by the ion bombardment.

Although the transconductance of E-mode HEMTs is smaller than that of D-mode HEMTs, its profile over the gate bias is relatively flat within a wide gate swing (from 1 V to 4 V), indicating good input-output linearity. The dc output characteristics of the E-mode HEMTs are plotted in Fig. 3, the maximum output current at 2.5V gate bias is about 220 mA/mm. On wafer small-signal RF characteristics were performed from 0.1 to 39.1 GHz on the 100-µm wide HEMTs at V_{DS} = 12 V. As shown in Fig. 4, the maximum current gain cutoff frequency (f_T) and power gain cutoff frequency (f_{max}) are 7.1 and 22.3 GHz for E-mode HEMTs and 8.5 and 29.7 GHz for D-mode HEMTs, respectively.

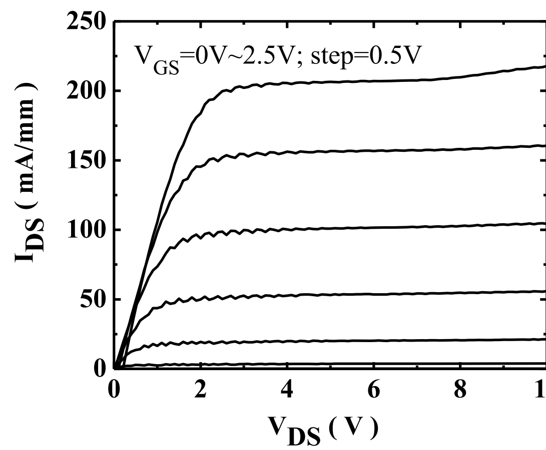

Fig. 3 DC output characteristics of E-mode HEMTs with a gate length of 1 µm. The gate-source spacing is 1 µm and the gate-drain spacing is 2 µm.

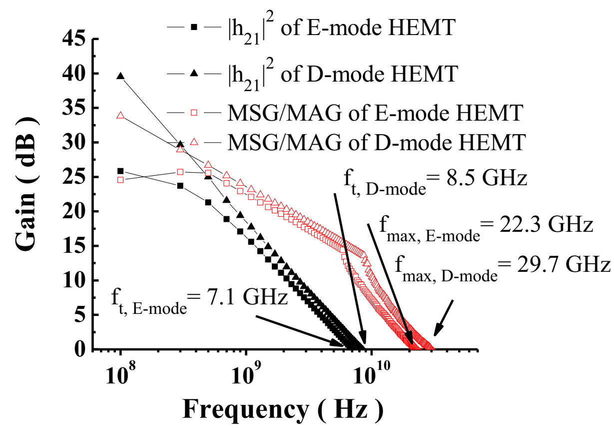

Fig. 4 Small-signal RF characteristics of D-mode and E-mode HEMT with a gate length of 1 µm, measured at bias V_{DS}= 12 V, V_{GS}= -1.4 V for D-mode HEMT and V_{DS}= 12 V, V_{GS}= 3.0 V for E-mode HEMT.

Distribution profile of F ions: SIMS measurement

The Varian CF3000 ion implanter is designed for high energy ion implantation. However, the thickness of AlGaN barrier is around 20 nm, which is too thin to stop the high energy fluorine ion at the barrier layer. Therefore, additional silicon nitride layer (80 nm thick for this experiment) is deposited as the energy-absorbing layer to prevent the majority of fluorine ions from being implanted into the channel. Otherwise, the F ions (considered as impurities) in the channel can significantly reduce the channel electron mobility as well as the transconductance of the transistors. The fluorine distribution profile was measured by secondary-ion-mass- Spectrometry (SIMS), as shown in Fig. 5. The high fluorine counts in AlGaN barrier layer compared to that in silicon nitride layer may be due to the different F ion yield (the fraction of sputtered atoms that are ionized) in silicon nitride and GaN based material. Fluorine atoms in the silicon nitride are presented in the Si-F bonds [10]. However, the fluorines in AlGaN or GaN are believed to be stand-alone negatively charged [4, 11, 12], and can be easily detected in SIMS. The high SIMS sensitivity of fluorine in AlGaN/GaN structure provides the evidence that supports the assumption of the negative charge state possessed by the fluorine ions.

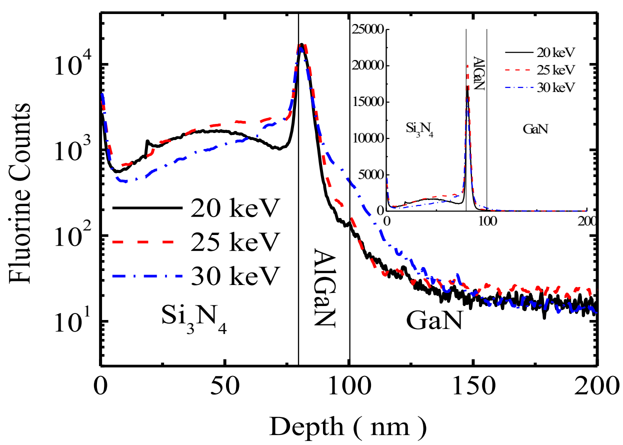

Fig. 5 Fluorine profiles measured by Secondary-Ion-Mass-Spectrometry (SIMS) of in Si_3N_4/AlGaN/GaN structure implanted with different energy (20 keV, solid; 25 keV, dash; 30 keV, dash and dot). The inset shows the profiles in linear scale.

The fluorine distribution profile is also confirmed with the SRIM (Stopping-and-Range-of-Ions-in-Matter) simulation [13], as shown in Fig. 6 (a-c). The parameters of each layer are set to be best match of the real sample. The density of PECVD-grown silicon nitride can not be measured precisely and is set to be 2.3 g/cm^3.

The simulation results are plotted in Fig. 6. With low energy ions (e.g. 20 keV), most of fluorine ions are incorporated in the Si_3N_4 layer, suggesting long implantation time. At higher energy (e.g. 30 keV), the F incorporation in AlGaN is efficient, but large amount of F ions also enter the channel region. 25 keV was chosen as the energy for our first experiment and was proven to be effective.

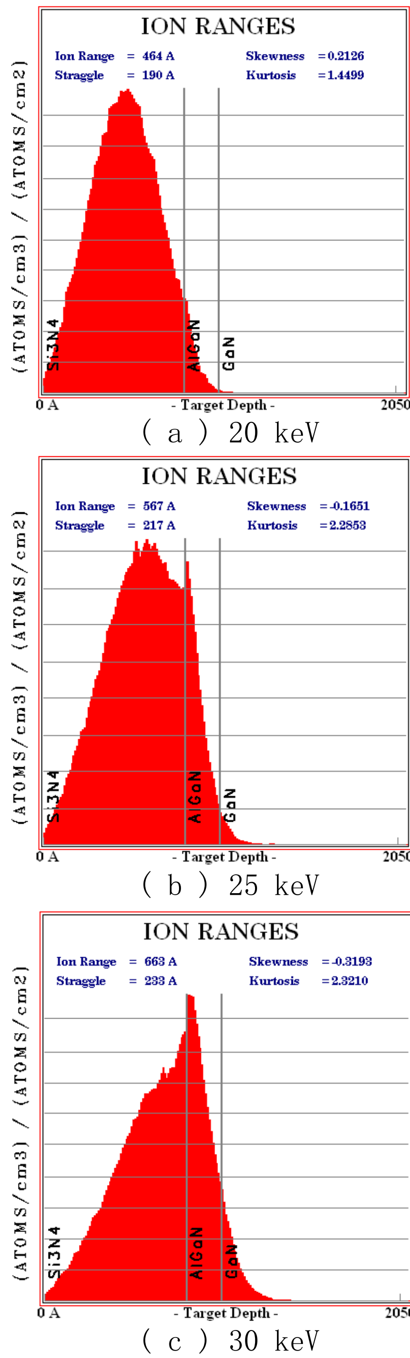

Fig. 6 Ion distribution profile of different $^{19}F^{+}$ ion implantation energy, (a) 20 keV, (b) 25 keV, (c) 30 keV in structure of $Si_3N_4/Al_{0.26}GaN_{0.74}/GaN$ (80/20/100 nm).

Conclusion:

The fabrication technology for enhancement-mode AlGaN/GaN HEMTs using standard fluorine ion implantation has been developed. A Si_3N_4 layer is used as the energy-absorbing layer for the high energy (~25 keV) ion implantation and enables the effective incorporation of negatively charged fluorine ions in AlGaN barrier. SIMS measurement and SRIM simulation both confirm that the fluorine ions are mainly distributed in the AlGaN barrier layer with a small fraction penetrating into the channel and buffer layer. The fabrication process also allows the monolithic integration of E/D-mode HEMTs for high performance digital/analog integrated circuits.

Acknowledgement

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ACRONYMS

AlGaN/GaN HEMTs: AlGaN/GaN High Electron Mobility Transistors
E-mode HEMTs: Enhancement-mode HEMTs
D-mode HEMTs: Depletion-mode HEMTs
SIMS: Secondary Ion Mass Spectrometry
SRIM: Stopping and Range of Ions in Matter
MOCVD: Metal Organic Chemical Vapor Deposition
ICP-RIE: Inductively Coupled Plasma Reactive Ion Etching
PECVD: Plasma Enhanced Chemical Vapor Deposition