Impact of gate metal fringe removal on small signal RF gain of AlGaN/GaN HEMTs

R. Behtash[1], J.R. Thorpe[1], S. Held[1], D. Schrade-Köhn[2], H. Blanck[1]

[1]United Monolithic Semiconductors, Wilhelm-Runge-Strasse 11, 89081 Ulm, Germany
[2]University of Ulm, Institute of Electron Devices and Circuits, 89081 Ulm, Germany
Reza.Behtash@ums-ulm.de. Tel.: +49 731 505 3077

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Abstract

In this paper a simple and applicable process step to improve the small signal RF gain of AlGaN/GaN-HEMTs is presented. By removing the gate metal fringes at the gate head of the devices the gain drain capacitance is reduced by an average of 30% at V_{DS}=40V. This results in an averaged gain improvement of 1.5dB at 10GHz. The presented process step can be easily implemented in an existing process flow.

I. INTRODUCTION

Due to the high breakdown voltage, high carrier density, high saturation velocity and because of the excellent thermal conductivity of SiC substrates AlGaN/GaN high electron mobility transistors (HEMTs) are very attractive for high frequency and high power applications. While the GaN technology has reached the necessary maturity to enter the market for L and S band applications there might be still some limitations regarding the RF gain of AlGaN/GaN-HEMTs in order to use them also at higher frequencies. In recent years there have been several reports on RF gain improvement of AlGaN/GaN HEMTs by modifying the epitaxial structure, mostly by aggressive reduction of the barrier thickness [1,2]. These epitaxial modifications often require an adaption of the process modules to the new epitaxy. In parallel it would be also very interesting to find methods from the processing point of view to improve the gain of the devices. These process modifications should be applicable for production and easy to implement. In this paper we report on such a method to reduce the feed-back capacitance (C_{GD}) of the devices by removing the gate metal fringes at the gate head.
The gate metal fringes which are a consequence of non-idealities during the evaporation of the gate metal increase the parasitic capacitances. The removal of the gate metal fringes and the reduction of the feed-back capacitance result in up to 1.5 dB more small signal gain at V_{DS}=40V and 10GHz.

II. TECHNOLOGY AND FABRICATION

The layer structure consists of a GaN cap layer and an undoped AlGaN barrier layer grown on a GaN buffer. The layers were grown on a 3" semi-insulating 4H SiC substrate by MOVPE. For the fabrication of the ohmic contacts a metallization based on Ti/Al was utilized. The isolation was done by ion implantation. A silicon nitride assisted gate module was used in order to achieve the necessary yield on large periphery devices for power applications. According to this processing scheme 0.25µm gate foot openings are defined in the nitride by electron beam lithography and then dry etched. In a second step the gate head is realized. While this gate module delivers excellent yield it has a big drawback.

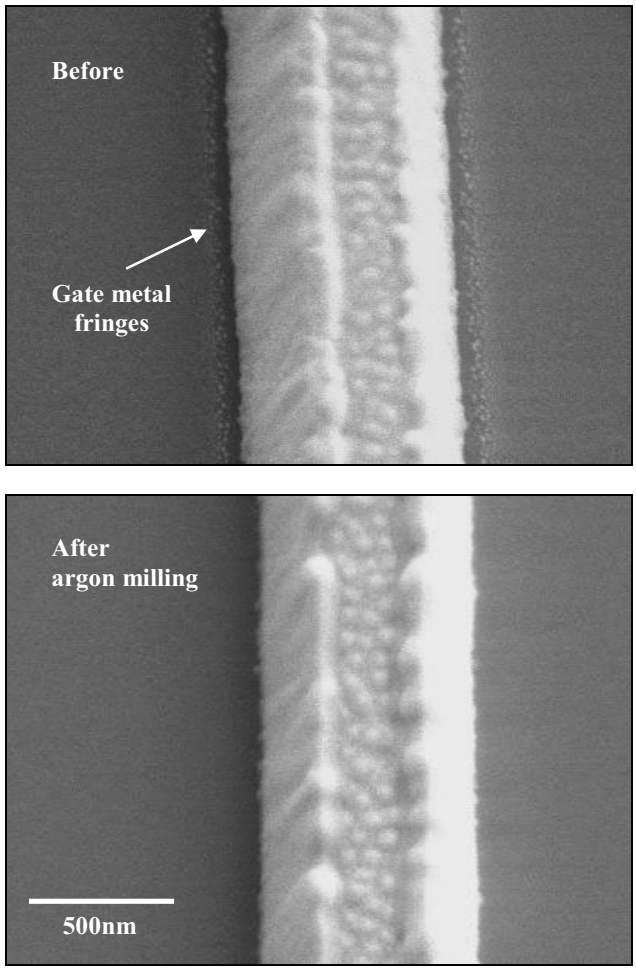

Figure 1: SEM pictures of the Ni/Au gates with gate metal fringes (top) and after the removal of the gate fringes by argon milling (bottom).

The gate head sitting directly on the silicon nitride results in increased parasitic gate drain capacitance and therefore in reduced gain. This parasitic capacitance is even higher when gate metal fringes are formed during the Ni/Au gate metal evaporation. The upper SEM picture in Figure 1 shows the gate metal fringes at the gate edge. The fringes are mainly the consequence of two non-idealities during the Ni/Au evaporation: the limited distance between the wafer and the crucible and the finite dimension of the crucible compared to a point source. The gate metal fringes don't contribute to the gate metal conductivity but increase the gate drain capacitance. Since dry etching of gold is not possible (a dry etching approach would only result in a redeposition of gold residues over the whole wafer) it was decided to apply argon milling to remove the fringes. Therefore after the gate lift-off the wafer was put into an evaporation tool and a standard argon milling was carried out. The result is illustrated in the lower SEM picture of Figure 1. An EDX analysis after the argon milling revealed that there is no more Ni or Au left at the gate edge on the silicon nitride surface.

III. Impact on Small Signal Parameters

The impact of the gate metal fringes removal was studied using 2x40µm PCM devices. Small-signal parameters of several PCM devices with different geometries (different drain source dimensions and devices with and without source-terminated field plates) have been measured at the bias point V_{DS}=40V and I_D=50mA/mm. Figure 2 shows the gate drain capacitance C_{GD} extracted at this bias point. For the standard wafer without gate fringes removal two groups of devices can be identified: devices with and without source-terminated field-plate. In both cases the gate drain capacitance is reduced by an average of 30 percent on the wafer with argon milling.

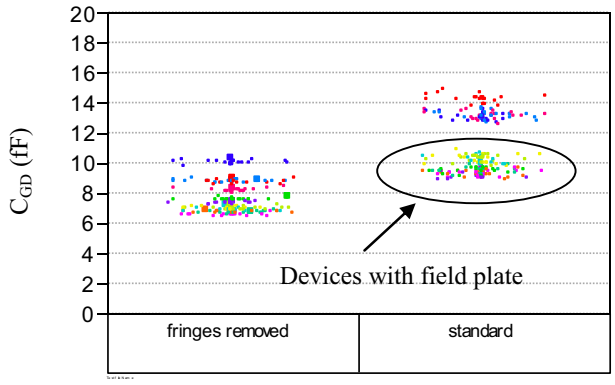

Figure 2: Trend chart of the gate drain capacitance of 2x40µm PCM devices with different geometries on two wafers with and without gate fringes in the bias point V_{DS}=40V, I_D=50mA/mm.

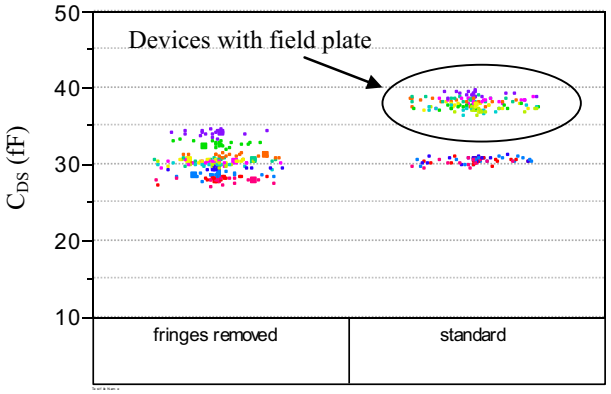

Figure 3: Trend chart of the drain source capacitance of 2x40µm PCM devices with different geometries on two wafers with and without gate fringes in the bias point V_{DS}=40V, I_D=50mA/mm.

There is also a positive impact on the output capacitance C_{DS} as displayed in Figure 3. In this case a significant impact is seen only for devices with field plate. The output capacitance is reduced by an average of 15 percent.

The impact of the reduction of the parasitic capacitances on the small signal gain is shown in Figure 4. In this trend chart the MSG/MAG of the devices in the bias V_{DS}=40V and I_D=50mA/mm can be seen for 3 different frequencies. At 2 and 10 GHz MSG is improved by an average of 2dB and 1.5 dB, respectively. The situation is different at 18GHz. At this frequency some device types have even less gain on the wafer with argon milling compared to the standard wafer. These device types are the ones with a bigger gate drain distance. Further analysis of the data revealed that these devices are already in the MAG region at 18GHz. This observation is confirmed by the trend chart of the k-factor in Figure 5. It can be seen that devices on the wafer with argon milling (fringes removed) have an earlier MSG/MAG transition frequency. The reason for that is a higher gate resistance on this wafer. Obviously too much gold is removed during argon milling. In order to avoid this problem two measures are now under investigation:

- The argon milling process is not optimized yet and too much gold is removed. According to AFM measurements it would be sufficient to remove 20nm gold in order to remove the thin gate fringes. In this way the increase of the gate resistance is reduced.

- The increase of the gate resistance can be compensated by increasing the thickness of the gate metal. The gate fringes are mainly formed at the beginning of the evaporation and their growth

rate is significantly reduced as the total metal thickness increases.

IV. Conclusions

An easy and applicable process step has been presented in order to improve the gain of AlGaN/GaN-HEMTs from the processing point of view. By applying argon milling in an evaporation tool gate metal fringes have been removed. This leads to a reduction of the gain drain capacitance by an average of 30% and to a reduction of the source drain capacitance by an average of 15% for devices with field plate. At 2 and 10GHz MSG is improved by an average of 2dB and 1.5dB, respectively. Since the argon milling process is not optimized yet too much gold is removed leading to an increase of the gate resistance and an earlier MSG/MAG transition. Investigations are now under way in order to optimize the process by reducing the argon milling time and/or increasing the gate metal thickness.

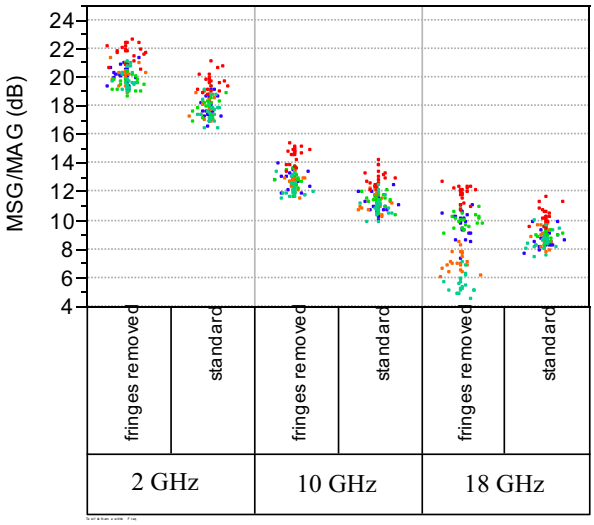

Figure 4: Trend chart of MSG/MAG of 2x40µm PCM devices with different geometries on two wafers with and without gate fringes in the bias point V_{DS}=40V, I_D=50mA/mm for three different frequencies.

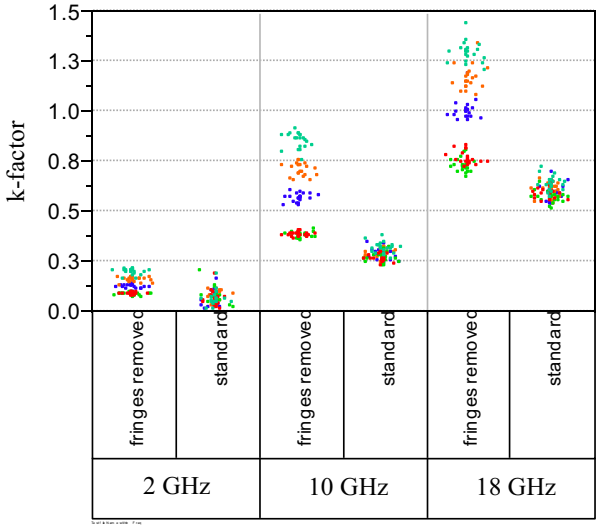

Figure 5: k-factor of the 2x40µm PCM devices with different geometries on two wafers with and without gate fringes in the bias point V_{DS}=40V, I_D=50mA/mm for three different frequencies.

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Acronyms

HEMT: High electron mobility transistor
AFM: atomic force microscope
MSG: most stable gain
MAG: most available gain
PCM: process control module
EDX: energy dispersive X-ray spectroscopy