Elimination of Yield Loss Due to Rogue Polyimide Vias

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Abstract

Polyimides are high performance polymer dielectrics commonly used in III-V semiconductor fabrication. These have a desirable planarizing property and have good dielectric and thermo-mechanical properties, such as low dielectric constant, low stress, high modulus and chemical resistance. The planarizing characteristics of polyimides are beneficial and useful when the substrate has significant topography, such as gallium arsenide (GaAs) heterojunction bipolar transistor (HBT) Power Amplifier (PA) devices, which have deep mesas. However, dry etching of polyimides can be a challenge due to lack of etch selectivity with photoresist and a tendency of polyimides vias to become enlarged during plasma processing, a large overetch cannot be used. In this paper, we discuss the case of "rogue" vias that did not open during the etching of polyimide used between Metal-1 and Metal-2, while the majority of the vias were open.

Introduction

Following the absolute necessity of product quality in semiconductor manufacturing, is the metric of yield, which fuels the strength of a company in the marketplace. Therefore, all systematic causes of yield loss must be aggressively investigated, so that robust solutions can be integrated into the process. To this end, the efforts of a vigilant yield engineering group combined with a cross-functional engineering team are invaluable to a company's success. This paper is an account of such an effort.

Our yield engineering group began noticing a repeating yield loss signature on multiple lots of our 4" GaAs HBT process. The yield loss was manifest in the corners of the stepped fields on the wafers. The circuits were failing for electrical opens during probe. Subsequent microscopic and SEM inspection revealed that the interlayer polyimide vias in the affected region were not completely cleared.

Investigation

Because the probe failures were defined by the stepping fields, the photo imaging process module became the prime suspect for the cause of the failures. The initial failure mechanism theory centered on the inability of the stepper to properly compensate for planar tilt at the affected field locations. The focal plane tilt created a poor exposure condition which left the photoresist via patterns improperly formed, which then prevented the plasma etch operation from completely etching the polyimide. A task team was assembled to investigate the problem.

In classical engineering fashion, the focus-tilt issue (as it was unceremoniously named) was evaluated using brainstorming techniques to formulate root-cause theories which would require validation. The items to investigate are listed in Table I.

TABLE I
PARAMETERS AFFECTING FOCUS-TILT

Stepper focus system operation
Resist thickness uniformity
Polyimide thickness uniformity
Wafer backside contamination
Stepper chuck contamination
A recent photoresist change for the polyimide via layer

Naturally, the photoresist change was immediately suspect. It is generally logical to suspect recent process changes when problems occur. In this instance, the chemistry change was unavoidable, as the previous resist had been discontinued by the vendor. Performance testing of the new resist resulted in similar CD's, profiles, and etch-rates as the original resist. Evaluation results of initial production lots processed with the new resist indicated that device performance was equivalent to devices using the old resist. Increased develop times were also evaluated, but no improvement to the closed via yield loss could be achieved. Based on these data points, the new resist was considered as having no impact on the yield loss problem.

The uncertainty of photoresist and polyimide film thickness uniformities was also quickly dismissed, as current and historical data revealed that the coat processes were well behaved. However, because the data was collected from silicon test wafers, which are much flatter than the GaAs production wafers, doubts lingered whether or not film thickness uniformity issues might contribute to

the focus-tilt problem. The investigation moved on, expecting to find lower hanging fruit.

It was difficult to separate wafer backside contamination from stepper chuck contamination, as the former precipitates the latter. Stepper chuck cleaning procedures were already employed, in abundance, to mitigate the focal plane exposure defects observed on a critical masking layer, caused by contamination being transferred onto the chucks from wafers with dirty backsides. These same cleaning procedures were temporarily begun for the Polyimide Via (PV) layer as a containment action, pending the successful elimination of the wafer backside contamination. The weakness of this approach is that after the chuck has been thoroughly cleaned and tested, the very next wafer processed has the potential to contaminate the chuck once again.

Wafer backside contamination has been a habitual problem, with flare-ups being associated to specific events which could be remedied with relative ease. The main sources of this contamination are the metal lift-off and resist coat processes. The problems inherent with these processes have received substantial scrutiny, leading to remedial repairs, which have reduced the systematic occurrences of contamination. Regular maintenance of the parameters affecting the cleanliness of the processes, listed in Table II, remain as sentinels to wafer quality.

TABLE II
PARAMETERS AFFECTING WAFER BACKSIDE CLEANLINESS

Lift-off Process	Resist Coat Process
Nozzle position	Backside rinse nozzle position
Solvent pressure	Backside rinse flow rate
Solvent temperature	Knife-edge position
Filter change frequency	Exhaust flow
Nozzle cleanliness	Hot plate cleanliness
	Chuck cleanliness

Having determined that the parameters affecting wafer backside contamination had been properly adjusted; -- without producing a significant reduction of the focus-tilt yield loss -- the investigation continued on to the stepper. Again, wafer backside contamination was not totally dismissed as a factor of the yield loss issue, only that is was not the main factor.

Another note is that although this investigation is being reported in serial fashion, the actual efforts were conducted in a parallel fashion by the varied members of the task team. This approach is desirable when a problem needs a solution in a timely manner.

The Canon-i3 steppers utilize a five-point focus detection system to compensate for field-by-field focus and tilt. The detectors are normalized by measuring a set number of reticle fields on the first wafer in a lot tilt pattern offset check (TPOC). Subsequently, deviations from the standardized values trigger an independent focus/tilt correction at every exposure field. This function is necessary for a non-planar fabrication process on wafers which are bowed due to thin-film stresses.

Because of the bowed nature of the GaAs process wafers, the integrity of the stepper TPOC had previously been improved by using sample fields in the center of the wafer, which are the flattest portion of the wafer. This technique improves the tilt compensation around the perimeter of the wafer, as one side of the wafer slopes in the opposite direction of the slopes on the other side of the wafer. Contamination hotspots have the potential to adversely affect the normalization of the TPOC, illustrating the associative character of the problem causes being investigated.

Testing revealed that the signal strength of the five focus channels were not adequately matched on the steppers assigned to the PV layer, which could cause an inconsistency in the focus-tilt measurements. The elements of the focus system were replaced, repaired, and/or adjusted. This single action had the most profound reduction on the focus-tilt yield loss issue than any of the other potential root-causes considered. However, it's highly probable that all of the activity (improvements, repairs, etc.) contributed to the yield improvement.

It appeared that the problem had been solved, but alas, the celebration was short-lived. The yield loss due to closed polyimide vias disappeared for a couple of weeks, only to return. However, the effect signature had mutated. The field corner yield loss effect was no longer prominent, and the closed polyimide vias were limited to a seemingly random selection. The term "rogue via" was applied to this phenomenon.

Rogue Vias

The rogue vias only appeared in the smallest vias in the circuit, while the larger vias were normally sized. Rogue vias were also discovered adjacent to good vias of the same dimension. Several discussions on the problem led to the action of increasing via dimensions on the reticle. Initial tests showed promise, so a plan was devised to modify the PV reticles of all the high runner devices.

A significant decrease in the yield loss due to the rogue via was observed, but it was disappointing that the problem had not been completely eliminated. Another round of investigations was in order, with the plasma-etch engineers joining the task team.

The plasma etch tools used for the polyimide etch, generate the same etch rate for polyimide as the photoresist mask. It is therefore necessary to have a sufficiently thick resist film to cover the topography so that the resist is not

completely eroded during etch. Under isotropic etch conditions, the polyimide sidewall profile will replicate that of the photoresist masking layer. With a process requirement to have sloped polyimide via sidewalls, it was necessary that the photoresist process be engineered to produce the desired profiles. Setting the via sidewall using thermal reflow proved to be uncontrollable, so exposure defocus was selected to generate the sloped sidewalls. However, it created a problematic process due to a reduction of the effective process window.

The task team revisited the polyimide via photo process by running a focus-exposure matrix and obtaining FIB cross-sections of the sidewalls. Nothing untoward was observed relative to the exposure conditions in current use. The track hotplates became the center of attention as issues with the temperature calibration and surface cleanliness were encountered. These issues did not prove to be the smoking-gun, but the opportunity to improve PM practices was not lost.

Even though the rogue vias were not successfully duplicated in the photoresist pattern, they would still appear after the polyimide etch. Looking for a rogue via using an optical microscopic was proving to be difficult, which also meant that clues might be missed, causing the investigation to flounder, or worse, to be misdirected.

At first glance, it appeared that the rogue vias were plaguing only two or three devices, although these devices were the majority of the devices in the current fab inventory. Closer examination revealed that the rogue vias were occurring in the same location on each of the failed dies, though the locations were different for each device layout. A review of circuit layouts showed that the rogue vias were in close proximity to large capacitor structures. These capacitors are built with the polyimide etched away, so the rogue vias were positioned in a relatively small area of stand-alone polyimide. This key discovery provided information which generated the development of a new set of theories that could be explored.

A previously interesting and anomalous photo pattern image, Fig. 1 (from the initial qualification of the new photoresist for the polyimide via layer), provided the basis for the next promising theory. It appeared that the polyimide was contracting during the plasma etch, when the resulting feature was an isolated island. Discussions centered on the physical properties of the polyimide: was the polymer contracting due to film stresses being released or was the film improperly cured, adversely enhancing its behavior to the plasma etch environment.

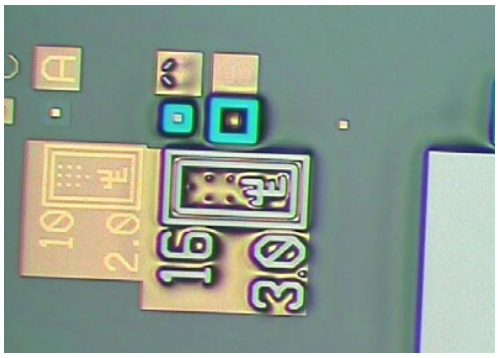

Figure 1 - Apparent contraction of Polyimide

The investigation then turned toward the polyimide coating and curing process, to determine whether or not it had shifted. The associated process parameters were checked: material batch number, hot plate temperature calibration, casting thickness, curing temperature calibration, and cured film thickness. It was found that all of the parameters were operating within the established processing limits. This information did not prove or disprove the theories about the physical behavior of the polyimide, but it did confirm that the polyimide process had not changed.

Fortuitously another focused ion beam (FIB) micrograph emerged, Fig. 2, which provided the next positive link in the investigation. The cross-section displayed a partially etched polyimide via with the photoresist virtually closed off. The width of the polyimide via indicated that the photoresist was initially open and sized correctly. During the course of the plasma etch, the photoresist flowed itself closed. The new resist does indeed seem to play a major role in this rogue via problem.

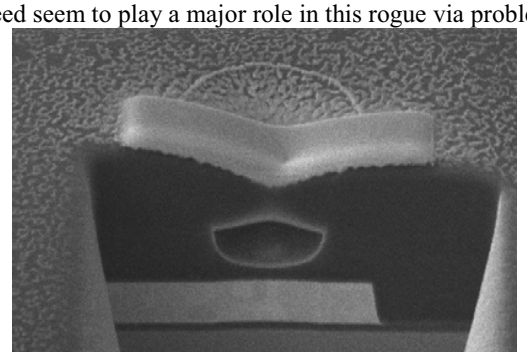

Figure 2 – Photoresist flow during Polyimide Etch

The rogue via problem had never been encountered with the old photoresist process, so it was evident that the new resist had different performance parameters that had not been discovered. Again the photoresist process was evaluated in terms of varying the softbake time and temperature, against the theory that excess solvent in the photoresist was allowing the patterned image to flow from elevated temperatures encountered during the plasma etch.

None of the conditions tested facilitated any reduction in the appearance of rogue vias.

Meetings continued, searching for theories on how the photoresist was experiencing an elevated temperature environment. Attention turned toward the plasma etch tools, which generates heat during the etch process. To prevent a wafer from heating up during the process, the wafer chuck is cooled with chilled water. The temperature of the chuck has never exceeded the process limits.

Commonality studies revealed that a single plasma etch tool was processing the lots with the rogue via problem. The etch tool field service engineer (FSE) was called in and requested to determine the health of the tool, concentrating on the chuck cooling function. Using a wafer with temperature measurement tabs placed on it, the FSE found that some locations on the wafer were reaching temperatures in excess of 140° C, which will easily flow the photoresist. These locations corresponded to the general areas on the wafer where the rogue vias were observed. The tool temperature data that was thought to be in control, actually came from the chuck and not the wafer.

Upon further investigation, it was discovered that the wafer chuck was badly worn to the point that the wafer was not making uniform contact. The lower electrode (which includes the chuck) was replaced and the polyimide etch tests rerun. The wafer temperatures were reduced and the rogue vias were no longer present. The root-cause of the rogue vias had finally revealed itself. The necessary testing for the etch tools to monitor the chuck cooling was immediately included in the PM procedures.

Conclusion

The closed via yield loss problem had been incrementally improved by each of the process improvements made during the course of the investigation. But misunderstood data had hidden the health of various process modules, necessitating that the second order causes be remedied before the main cause of the rogue vias could be discovered. Additional robustness was built into the process through design rule restrictions being implemented concerning the placement of the polyimide via.

There may be several solutions to a given problem which will provide a return to normal processing conditions. These solutions may be simple and obvious, difficult to discover, or driven by limitations of equipment, process, or budget. Some of these solutions may not forestall the reappearance of the problem. The best solution, however, is generally reached through the collaborative efforts of a team comprised of members representing the various aspects of the process under review. Following a structured methodology of problem solving, such as 5D or 6-sigma, will provide the team with the necessary tools to cultivate ideas and explore theories, which in turn leads to successful solutions of otherwise daunting problems.

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