Electrochemical Etching of Ion Implanted Channel Regions in GaAs

J. Crites, J. Dilley, S. Kittinger, W. Pickens, W. Polhamus, M. Balzan, M. Drinkwine
Cobham Blacksburg, 3155 State St., Blacksburg, VA 24060
Phone: 540 443-2800, E-mail: james.crites@cobhamdes.com

Abstract

Electrochemical etching or corrosion of GaAs in the vicinity of metal contacts is a well known phenomenon in the compound semiconductor device and IC manufacturing industry. Corrosion of GaAs has been most frequently reported for situations where wafers with bare regions GaAs and metal contacts are exposed to de-ionized water for extended periods of time. The corrosion typically manifests only in close proximity to the edge of the metal contacts. Recently we determined that some MSAG wafer losses, characterized by FETs with abnormally low drain current under positive gate bias, were caused by electrochemical oxidation and etching of the implanted near-surface region of the FETs. Investigation traced the source of the problem to a dump rinse step where oxidation was taking place followed by etch removal of the oxide in the FET channel at a subsequent acid-exposure step. This paper will discuss some of the abnormal corrosion behavior we observed in comparison to that reported in the literature. Discussion will also be presented regarding beneficial FET attributes that can be obtained from a controlled amount of corrosion/etching in the process sequence that was causing the problem that led to this investigation.

INTRODUCTION

Although the MSAG GaAs IC fabrication process (Fig 1) emphasizes the use of dry processing and protective dielectric films, it nevertheless still uses wet processing at several operations, with exposure of bare GaAs to de-ionized (DI) water and acids early in the process sequence.

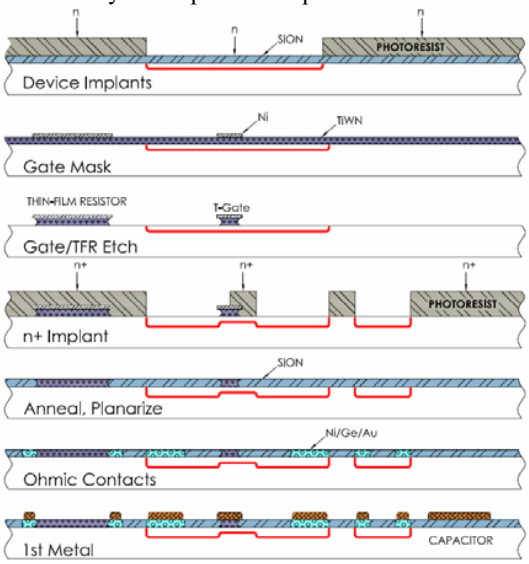

Figure 1. MSAG FET fabrication process flow up through first metal..

Furthermore, as also shown in Figure 1, a standard feature of the MSAG process, in comparison to other FET IC technologies, is the lack of a gate recess. Therefore, with this planar-processing approach, the GaAs topology is featureless extending from the source to the drain as shown in the SEM FET cross section in Figure 2.

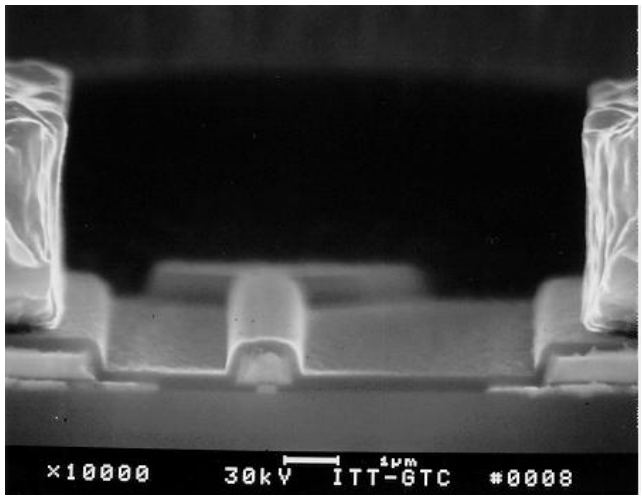

Figure 2. SEM cross section picture of MSAG FET showing the planar structure without a recessed gate.

Recently we observed production MSAG wafers exhibiting abnormal dc parametric FET behavior, characterized predominantly by a drop in Ipeak without a corresponding change in Idss or Vt, as depicted in Figures 3 and 4, and resulting in yield loss at the Process Control Monitor (PCM) screening point in the process.

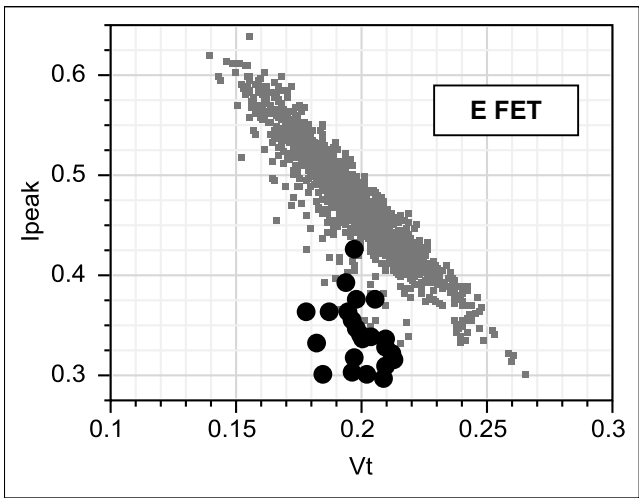

Figure 3. Ipeak vs Vt shows the abnormal wafers (black data) with much lower Ipeak than standard wafers (grey data) with the same Vt.

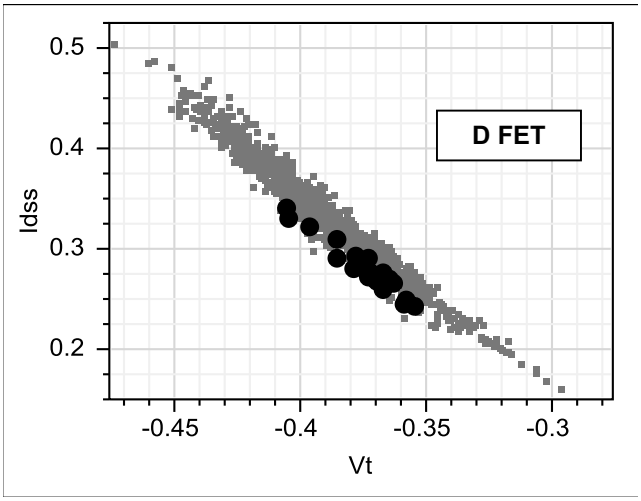

Figure 4. Idss vs Vt shows the abnormal wafers (black data) have approximately the same Idss as standard wafers (grey data) with the same Vt.

Investigation and failure analysis of the wafers with abnormal PCM characteristics traced the source of the abnormality to unintentional removal of GaAs in the channel region of the affected FETs, as shown in an SEM cross section picture of a worst-case FET (Fig 5).

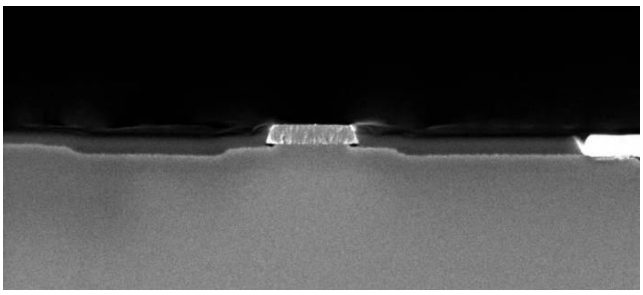

Figure 5. SEM cross section picture of partially-processed MSAG FET exhibiting the corrosion problem. Note the lack of trenching near the metal contacts and the smooth etched surface. The amount of GaAs corrosion and removal varies laterally and correlates with the implant parameters used in the different regions. GaAs has not been appreciably removed under the gate electrode accounting for the unchanged value of Vt.

The root cause of the abnormality was later determined to be from extended exposure to DI water at a process step where the bare GaAs channel was exposed. Based on "common knowledge" about GaAs corrosion and etching in aqueous environments, this result may not have been totally unexpected for most practitioners in the CS IC industry. However, long-time experience with the MSAG process had never shown a marked sensitivity to GaAs corrosion at the particular operation that was identified as the root cause of the problem, nor is high sensitivity to corrosion/etching to be readily expected there, due in part to the fact that implants had not yet been "activated" at this point in the process to produce normally-conductive n-type material.

Follow up investigation showed that there is a small corrosion sensitivity to DI water exposure at this step in the process but that it behaves in a fashion somewhat different than what is typically reported in the literature. In addition, as a result of the problem-solving investigation it was found that a small, controlled amount of GaAs removal in the channel region at the operation where the problem occurred has beneficial effects, such as reduction in leakage current, without adversely affecting the primary parametric characteristics or performance of the MSAG FET. This last finding is being used to pursue additional optimization of MSAG FETs for improved performance, further extending the application of MSAG technology, with particular emphasis on high-voltage operation.

BACKGROUND

Unintentional etching and/or corrosion (a chemical or electrochemical reaction between a material and its environment that produces a deterioration of the material and its properties) of GaAs in aqueous solutions, including high-purity DI water, has been observed and reported at least as far back as 1981 [1]. Many groups have reported on the phenomenon of GaAs corrosion, especially due to DI water exposure [2-8]. M. Hagio [3] has explained the corrosion process as being facilitated by oxygen dissolved in, and reacting with, the DI water to form OH^- ions at the metal electrode, which then react with Ga and As to form Ga- and As-oxides. Although the general electrochemical mechanisms responsible for GaAs corrosion in DI water are understood, there is incomplete understanding of subtle differences observed and reported due to the fact that in practical applications there are many factors that influence the oxidation and dissolution reactions. Some of the key observations for GaAs corrosion (from the references cited above) are as follows:

1. The primary electrochemical reaction is galvanic and is facilitated by a metal in contact with the GaAs surface
2. The higher the galvanic potential difference between the metal in contact with the GaAs and the GaAs, the stronger the reaction
3. Galvanic corrosion of GaAs is observed in proximity to both ohmic and rectifying contacts
4. The corrosion process involves formation of Ga- and As-oxides which are typically soluble and removed in the aqueous solution where the corrosion is taking place, giving rise to etched regions or pits in the GaAs
5. In DI water, the reaction rate correlates with the amount of dissolved oxygen – higher amounts of dissolved oxygen produce higher reaction rates.
6. As a galvanic reaction, it is necessary for the GaAs to be conductive to enable efficient charge transfer (and by inference, the more highly conductive is the GaAs, the stronger is the corrosion reaction)
7. The corrosion or removal of GaAs is strongest close to the metal (due to IR voltage drop across the DI water electrolyte)
8. Trenches (several hundred angstroms deep) in the GaAs adjacent to the metal are commonly observed
9. In addition to trenching, the corroded surface of the GaAs further removed from the metal contact is typically rough and pitted at the microscopic level
10. The reaction is facilitated/enhanced by exposure of the material to light

When corrosion of GaAs, as described above, occurs in active device regions the obvious consequence is a change in device performance compared to devices without corrosion. Removal of GaAs material as a result of the corrosion process diminishes the current carrying capacity of the active region (e.g., source-to-gate "channel-access" region in a FET) thus degrading dc and RF parameters such as Ron, Ipeak, Idss, Gm, Ft, etc. for FETs. Therefore, it is common practice in GaAs IC manufacturing to avoid (or at least minimize) contact with DI water for process steps where bare GaAs is exposed on wafers with metal contacts and conductive (active) regions of GaAs.

OBSERVATIONS AND EXPERIMENTAL RESULTS

For the problem (and solution) reported here, we found some differences in behavior as compared to the typical observations reported in the literature for GaAs corrosion in DI water. Long-term experience with the MSAG process had never demonstrated any obvious corrosion effects arising from process operations where bare GaAs was exposed to DI water for modest durations – and therefore, the casual assumption was that the length of time in DI water did not really matter for our process. And, in particular, the part of the process sequence where the corrosion problem was found to originate for the abnormal-behavior wafers, involved GaAs wafers that had been implanted but not activated; therefore, corrosion at this point in the process was never considered an important concern due to lack of significant conductivity in the later-to-be-active device regions. Furthermore, immediately following DI water exposure, there was no indication of GaAs removal. In the follow up investigation, we observed, after extended soak time in DI water, a discoloration of the GaAs in implanted regions with metal contacts (Figure 6) – an indication that oxidation of the GaAs had taken place. Step-height measurements of these discolored regions showed no evidence of GaAs removal.

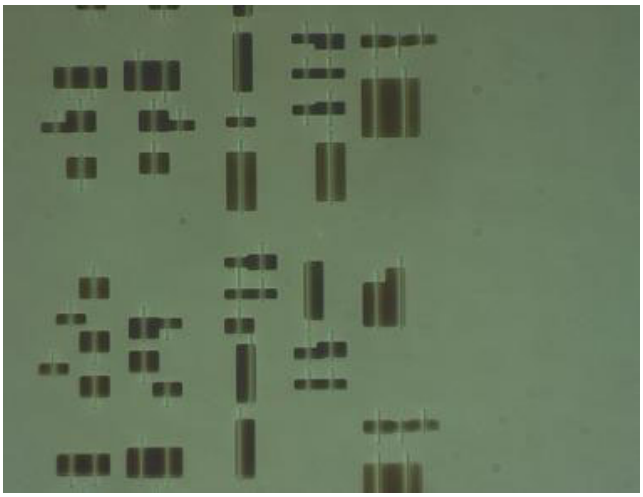

Figure 6. Optical picture of wafer after 120 minutes of DI water exposure. Only implanted regions with gate-metal contacts show discoloration, but material has not yet been removed. Evidence of etching shows up later after exposure to HCl.

In our observations we found three principal differences compared to other investigators: 1) No removal of GaAs-oxides during the DI water soak, 2) Affected regions were implanted but they had not been "activated" to produce normal conductivity, and 3) Upon removal of the DI-water-formed oxides at a later acid-dip step, the etched regions exhibited microscopically smooth features with no trenching near or adjacent to the metal contacts.

In summary, the experiments conducted as part of the root cause follow up investigation showed the following behavioral characteristics for GaAs corrosion at the process point of interest in the MSAG process:

1. As expected, the amount of corrosion correlates with length of time wafers soak in DI water: longer soak time, more corrosion
2. It is not necessary to anneal or "activate" the n-type implant to produce sufficient conductivity in the GaAs to facilitate corrosion. Most likely the implant damage produces conductive paths that are sufficient for the amount of charge transfer required in the corrosion process.
3. Larger amounts of corrosion took place in regions with higher n-type implant dose and energy as shown in Figure 3.
4. The type of metal in contact with the GaAs influences the corrosion rate. In fact, changes in the metal stack (we looked at TiWN, TiWN/Ni, and TiWN/Ni/Al) have an effect on the corrosion rate. Of the stacks we investigated, we found the full stack of TiWN/Ni/Al produced the most amount of corrosion.
5. The higher the amount of dissolved oxygen, the higher the corrosion rate. We were able to vary dissolved oxygen in the DI water over more than an order of magnitude and monitor corrosion rate. The highest oxygen concentration showed ~3 times higher corrosion rate than the corrosion rate for the lowest oxygen concentration of ~100ppB.
6. The corrosion process we observed did NOT involve appreciable dissolution of the GaAs oxide while the wafers soaked in the DI water. It was not until the DI-soaked wafers were placed in an HCl acid solution that the oxide removal was readily apparent.

PROCESS IMPROVEMENT

After identifying DI water exposure time as a contributing factor for device variability (and PCM yield loss in extreme cases), we proceeded with evaluation of key device parameters as a function of DI water soak time at the step in the process identified as the most sensitive to GaAs corrosion. Figures 7 and 8 show the results of split-lot experiments in which DI-water soak time was investigated over times ranging from "zero" to 40 minutes. Not surprisingly, the very long DI water soak time of 30 minutes showed excessive degradation of FET current as characterized by the Ipeak parameter. The low Ipeak values for 30 min soak time were similar to Ipeak values for the problem lots that initiated this investigation. Conversely, we observed that leakage (Ileak in Fig 8), was reduced (improved) for longer DI water exposure time, showing a stronger effect than that normally observed for Idss vs Ileak correlation. Furthermore, in our initial efforts to control the process better, the DI water soak time was

set to "zero" via strict enforcement of the manual loading/unloading process by the operators, with a consequence that wafer failures were subsequently observed for high FET reverse-bias leakage and higher-than-normal FET current. We therefore concluded that a small amount of GaAs removal in the surface region of the FET was more beneficial for leakage reduction than it was detrimental for current reduction. As an interim approach, a small amount of DI-water-soak-time has been specified as standard, resulting in improved FET parameter control and increased yield at the PCM screening point. Further process improvement is planned to provide better control of the small amount of GaAs etching required for optimum process control of PCM target values and improved yield.

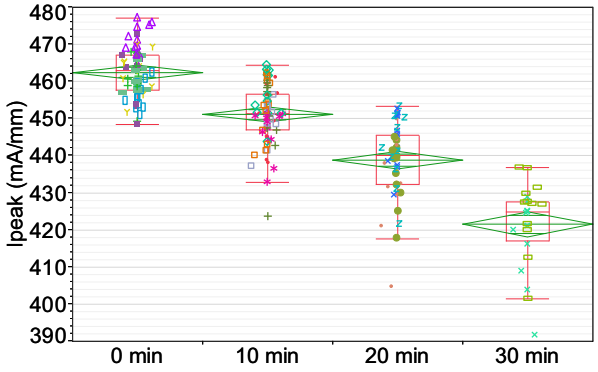

Figure 7. Results of split-lot experiment showing monotonic reduction in FET Ipeak for increasing soak time in DI water.

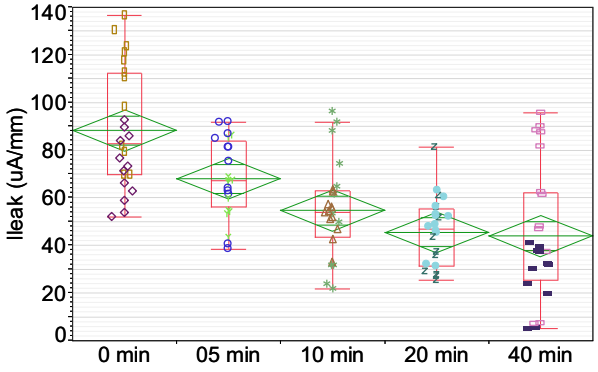

Figure 8. Results of split-lot experiment showing monotonic reduction in FET reverse-bias leakage for increasing soak time in DI water.

CONCLUSIONS

It is well known that conductive GaAs with metal contacts will corrode in DI water. We observed corrosion of GaAs, *which was implanted-but-not-annealed,* when exposed to DI water which contained a high concentration of dissolved oxygen. And, unlike other reports, dissolution of the oxide products produced during the DI water exposure did not take place until the wafers were subsequently exposed to an acid solution. Although extremely long time in DI water at key process steps where bare GaAs was exposed was found to be detrimental to FET performance, we found that short exposure times, resulting in removal of near-surface layers of GaAs, could be beneficial to device performance by decreasing reverse-bias leakage without significantly affecting primary device parameters such as Ipeak. This finding is being applied to reduce FET-parameter variability and is also being investigated as a possible path for achieving device performance improvement, particularly for devices where low leakage and high breakdown voltage are primary performance drivers.

ACKNOWLEDGEMENTS

Thanks to: M. Flora for performing special testing and data base support, J. Hylton for help performing investigations and experiments, and all the Cobham wafer fab operations personnel for their processing efforts in support of this investigation.

REFERENCES

[1] C.E. Weitzel, T.H. Miers, *IEEE Electron Device Letters*, vol. EDL-2, No.2, 1981
[2] C. E. Weitzel and T. H. Miers, *IEEE Trans. Electron Devices*, ED-29, 1982
[3] M. Hagio, *J. Electrochem. Soc.*, Vol. 140, No. 8, 1993
[4] M. Tsunotani, T. Ohshima, M. Sato, R. Shigemasa and T. Kimura, *1999 GaAs MANTECH Conference*
[5] I. Hallakoun, T. Boterashvile, G. Bunin and Y. Shapira, *2000 CS MANTECH Conference*
[6] J. Moore, H. Hendriks, and A. Morales, *2003 CS MANTECH Conference*
[7] H. Shen, L. Luu-Henderson, S. O'Neil, S. Tiku, T. Grayson, R. Ramanathan, *2004 CS MANTECH Conference*
[8] K. Cheng, *2009 CS MANTECH Conference*