High Performance InAlN/GaN HEMTs on SiC Substrate

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Abstract

In this work, we study the scaling characteristics of $In_{0.17}Al_{0.83}N$/GaN high electron mobility transistors (HEMTs). Scaling of both the DC and RF performance are studied as a function of InAlN thickness, gate recess and gate length to explore the design space of high frequency InAlN/GaN devices. Surface passivation by Al_2O_3 deposited using atomic layer deposition (ALD) is also investigated as an alternative to Si_xN_y passivation. The fabricated devices give record maximum drain current density and transconductance.

INTRODUCTION

InAlN-barrier high electron mobility transistors (HEMTs) have recently been proposed as an excellent candidate for high-power and high-temperature electronic applications [1, 2]. $In_{0.17}Al_{0.83}N$ can be grown lattice-matched to a GaN buffer, thus reducing the stress in the barrier layer, which is expected to improve the device reliability [3, 4]. Furthermore, an InAlN barrier has higher polarization and better thermal stability than traditional AlGaN barriers [1]. Due to the stronger polarization effects in InAlN, InAlN/GaN HEMTs show higher two-dimensional electron gas (2DEG) charge density in the channel with a much thinner barrier layer than in AlGaN/GaN HEMTs. This helps to improve the aspect ratio of the transistors for a given gate length and is very important for reducing short channel effects in high frequency HEMTs [5]. In addition, the higher 2DEG charge density in InAlN/GaN HEMTs also results in higher output current density and, potentially, higher power density [1, 6, 7, 8].

In this work, we study the scaling behavior of $In_{0.17}Al_{0.83}N$/GaN HEMTs as a function of InAlN thickness, gate recess and gate length to explore the design space of InAlN/GaN devices. Based on the knowledge from the scaling studies, we then fabricated devices that are optimized for high current and high transconductance. Surface passivation by Al_2O_3 is also studied as an alternative to Si_xN_y passivation. The fabricated devices give record maximum drain current density and transconductance.

SAMPLE STRUCTURE AND DEVICE FABRICATION

Three wafers of $In_{0.17}Al_{0.83}N$/GaN heterostructures are grown on SiC substrate using metal-organic chemical vapor deposition (MOCVD). After an AlN nucleation layer, 2 µm of GaN buffer is grown, which is followed by a 1.5 nm AlN interlayer, and the In_0lN barrier layer. The InAlN barrier thickness varies from 8.9 nm to 7 nm in the three different samples. Al compositions are measured by X-ray diffraction. The sheet resistance in the three samples are R_{sh}=230 Ω/□, 248 Ω/□, and 325 Ω/□ for barrier thickness of 8.9 nm, 7.4 nm and 7 nm respectively. These three samples are used to study the scaling behavior of the device characteristics. A fourth wafer with $In_{0.17}Al_{0.83}N$/GaN heterostructures and 1.5 nm AlN interlayer is also grown, which has a sheet resistance R_{sh}=220 Ω/□. Sample 4 shows the best electrical properties due to successful suppression of Gallium incorporation into the InAlN barrier and close-to-lattice-match growth on GaN. Figure 1 shows the detailed structures of the four samples.

Sample 1	Sample 2	Sample 3	Sample 4
$Al_{83}In_{17}N$ (8.9 nm)	$Al_{83}In_{17}N$ (7.4 nm)	$Al_{83}In_{17}N$ (7 nm)	$Al_{83}In_{17}N$ (6.9nm)
AlN (1.5 nm)	AlN (1.5 nm)	AlN (1.5 nm)	AlN (1.5 nm)
GaN (2um)	GaN (2um)	GaN (2um)	GaN (2um)
AlN Nucleation	AlN Nucleation	AlN Nucleation	AlN Nucleation
SiC substrate	SiC substrate	SiC substrate	SiC substrate

Fig.1 Sample structures: Samples 1, 2, 3 are used for the scaling study of the device characteristics. Sample 4 is used to fabricate devices optimized for high current density and transconductance.

Fig.2 Fabrication process. L_{DS}=1.5 µm, W_G=2×25 µm and L_G=50 nm to 350 nm in the fabricated devices.

The fabrication of the transistors starts with the deposition of a Ti/Al/Ni/Au multilayer for the ohmic contact formation. Cl_2/BCl_3 dry etching is then used for mesa isolation. Electron beam lithography defines the T-shape gate, which is formed by depositing a Ni/Au/Ni metal stack. The transistors are then passivated by 25 nm of high-k dielectric material, Al_2O_3, deposited using atomic-layer-deposition (ALD). The Al_2O_3 passivation improves the sheet resistance and the transconductance by up to 16% and 10% respectively while effectively removing dispersion. Transmission-line measurements (TLM) show sheet resistances of R_{sh}=220 Ω/□ and 206 Ω/□ in Sample 4 before and after passivation. Contact resistances in all samples are between 0.35 Ω•mm and 0.45 Ω•mm. All the devices have two gate fingers, with a total gate width of W_G=2×25 μm. The drain to source separation is L_{DS}=1.5 μm and the gate length L_G varies from 50 nm to 350 nm. Figure 2 shows details of the fabrication process. In addition, several devices were entirely defined with optical lithography and have L_{DS}=5 μm, L_G=2 μm and W_G=2×75.

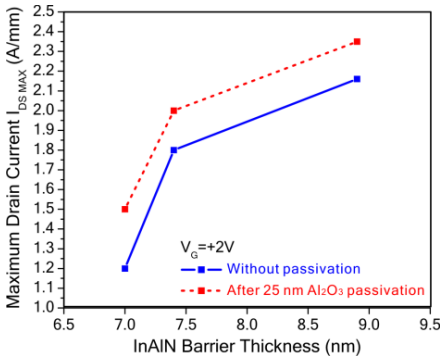

Fig.3 Scaling of $I_{DS,max}$ with InAlN barrier thickness (Sample 1, 2 and 3) before and after 25 nm Al_2O_3 passivation.

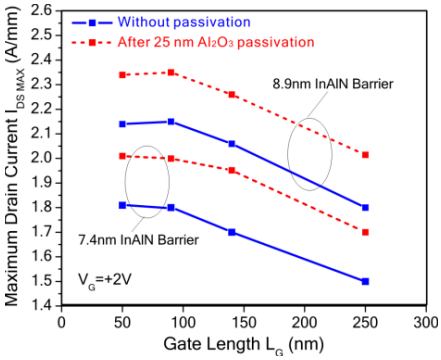

Fig.4 Scaling of $I_{DS,max}$ with gate length for both 8.9 nm and 7.4 nm InAlN barrier samples (Sample 1 and 2) before and after 25 nm Al_2O_3 passivation.

RESULTS AND DISCUSSION

A. Scaling of Device DC Characteristics The InAlN barrier thickness has a significant effect on the maximum drain current density ($I_{DS,max}$) [9,10]. Figure 3 shows that as barrier thickness increases from 7 nm to 8.9 nm, $I_{DS,max}$ increases from 1.5 A/mm to 2.36 A/mm. $I_{DS,max}$ also increases with decreasing gate length up to L_G =100 nm (Figure 4). Reducing L_G below 100 nm has little effects on $I_{DS,max}$.

Al_2O_3 passivation helps to improve the charge density in the 2DEG and hence reduce the sheet resistance. This reduction in sheet resistance increases the maximum current density by about 15-20% (Figures 3 and 4). This effect is stronger in samples with thinner barriers due to the higher effect of the surface potential in thin barrier devices.

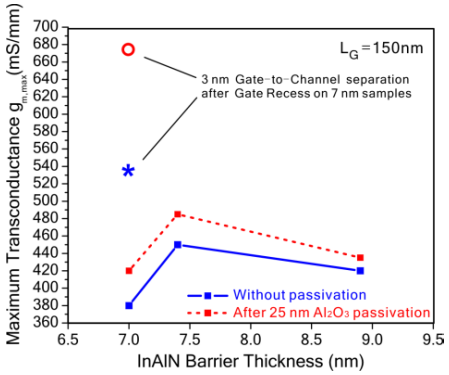

Fig.5 Scaling of $g_{m,max}$ with barrier thickness (Sample 1, 2 and 3). Solid and dotted curves: devices without gate recess before and after 25 nm Al_2O_3 passivation. Star and circle: devices with gate recess before and after 25 nm Al_2O_3 passivation.

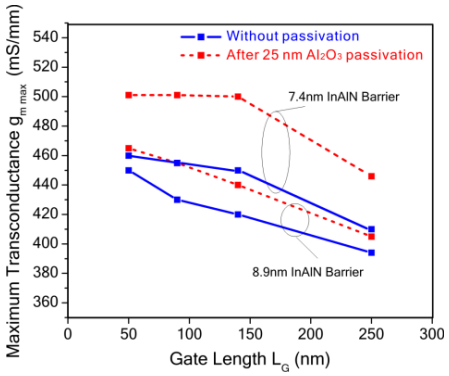

Fig.6 Scaling of $g_{m,max}$ with gate length for both 8.9 nm and 7.4 nm InAlN barrier samples without gate recess before and after 25 nm Al_2O_3 passivation.

Barrier thickness and gate length also have critical effects on the transconductance, g_m. Figure 5 shows that g_m has a maximum value in devices with a barrier thickness of 7.4 nm. For thicker barriers, electrostatic control worsens as gate is farther away from the channel, while for thinner barrier the charge density in the channel reduces, which increases the access resistances and reduces the extrinsic transconductance. $g_{m,max}$ also increases with decreasing gate length, possibly due to decreasing gate capacitances and higher electron velocity (Figure 6). Gate recess, which improves electrostatic control on the channel without

reducing sheet charge density in the access regions, can significantly increase transconductance. In a 150 nm gate length device on Sample 3, we obtained $g_{m,max}$ of 675 mS/mm (with $I_{d,max}$=1.5 A/mm) after recessing the gate to achieve 3 nm gate-to-channel separation [6].

B. Scaling of Device RF Characteristics Both the current-gain and the power-gain cut-off frequencies (f_T and f_{max}) of InAlN/GaN HEMTs scales well with gate length. On the 6.9 nm barrier sample with 83% Al (Sample 4), f_T increases from 25 GHz to 82 GHz and f_{max} increases from 73 GHz to 161 GHz as gate length reduces from 350 nm to 100 nm (Figure 7). The sample has 25 nm Al_2O_3 passivation and no gate recess.

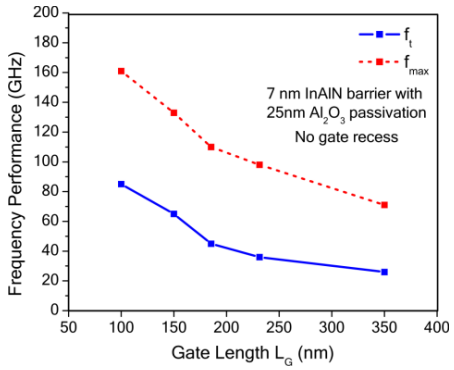

Fig.7 Scaling of frequency performance with gate length for Sample 4.

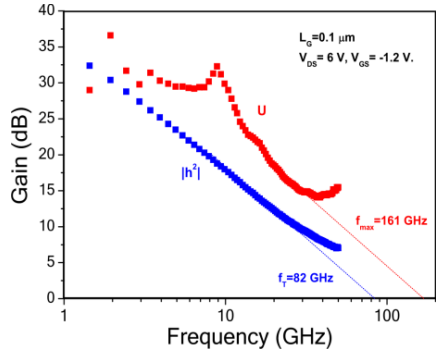

Fig.8 Frequency performance of a device on Sample 4 with L_G= 100 nm.

Figure 8 shows the frequency performance measurement data of a device with L_G=100 nm, which has f_T=82 GHz and f_{max}=161 GHz obtained by extrapolating measured data with a slope of -20 dB/dec using a least-square fit.

C. Record $I_{d,max}$ and $g_{m,max}$ With knowledge from the scaling studies permormed in the first three samples, we then fabricated devices on the fourth sample optimized for high current density and transconductance. A record current density of 2.5 A/mm at V_G=+2 V is obtained in Sample 4 in a device with L_G=100 nm (Figure 9). Figure 11 compares the current density of the devices demonstrated in this work with the state-of-the-art results found in literature. The highest DC current density reported until now for InAlN/GaN HEMTs is 2.3 A/mm with 13 nm $In_{0.19}Al_{0.81}N$ barrier, which also give 2.8 A/mm (circle on Figure 11) after removing the self-heating effect under pulsed conditions [1]. The state-of-the-art AlN barrier device (square on Figure 11) [11] also gives a maximum current of 2.3 A/mm. In addition, all AlGaN/GaN HEMT structures have lower current density than the best values in Figure 11 due to the weaker polarization effects in AlGaN barrier and hence lower charge density in the channel. Figure 12 compares the transconductance in the same devices. Before applying gate recess, the devices fabricated in this project have transconductance of 580 mS/mm. After reducing the barrier thickness between 3 and 4 nm by gate recess, the transconductance in the device with 150 nm gate length increased to 690 mS/mm (with $I_{d,max}$=1.4 A/mm), which to the best of our knowledge is also state-of-the-art.(Figure 10). For comparison, the highest transconductance reported so far in any nitride semiconductor was 635 mS/mm (with $I_{d,max}$=1.4 A/mm) in deep-recessed AlGaN/GaN HEMTs [12].

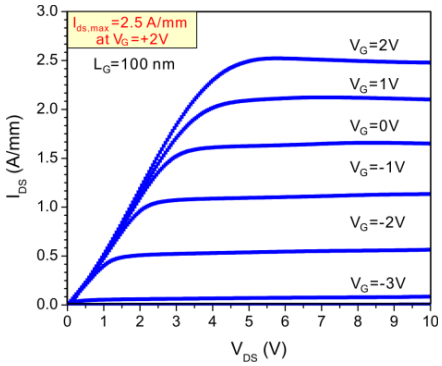

Fig.9 DC characterisitcs of 6.9 nm InAlN barrier device (Sample 4) with L_G=100 nm and record $I_{DS,max}$.

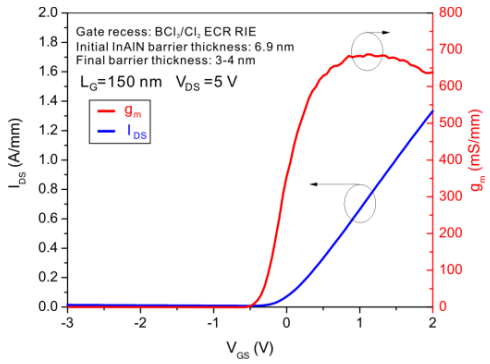

Fig.10 Transfer characteristics of 6.9 nm InAlN barrier device (Sample 4) with L_G=150 nm and record $g_{m,max}$.

D. Breakdown Voltage Figure 11 shows the breakdown voltage of devices with L_G =2 μm, L_{DS} =5 μm using both 2 terminal and 3 terminal measurements with 1 mA/mm criteria. The breakdown voltage increases with increasing barrier thickness. In the 8.9 nm barrier sample (Sample 1),

the breakdown voltage is 53 V and 63 V using the 2 terminal and 3 terminal methods respectively.

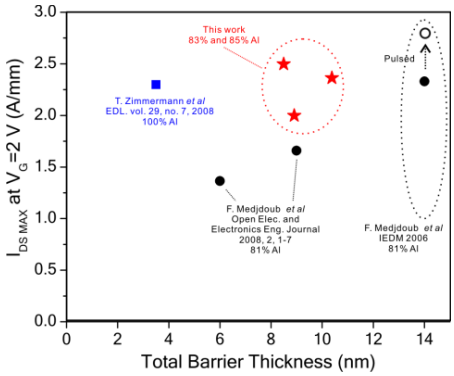

Fig. 11 Comparison of maximum drain current density obtained in this work with state-of-the-art devices in literature.

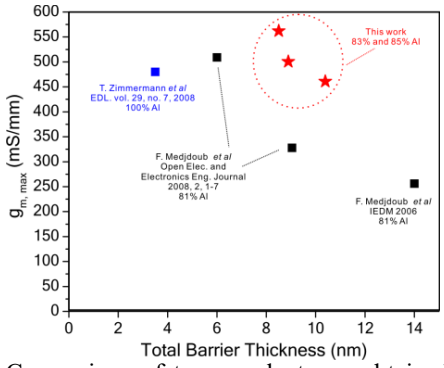

Fig. 12 Comparison of transconductance obtained in this work with state-of-the-art data in literature for devices without gate recess.

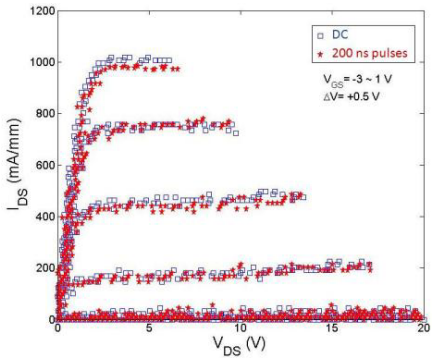

Fig. 13 Pulsed I-V measurement of a device on Sample 3. Al_2O_3 effectively suppresses dispersion.

Pulsed I-V measurements on Sample 3 show that Al_2O_3 passivation effectively suppresses dispersion (Figure 13). The gate pulse is 200 ns with 100 Ω load line [6].

CONCLUSIONS

In conclusion, we have investigated the design space of submicron InAlN/GaN HEMTs on SiC substrates with a thin Al_2O_3 passivation. Record current density and transconductance have been achieved. The reported device performance demonstrates the great potential of InAlN/GaN HEMTs as an alternative to AlGaN/GaN HEMTs for high-power high-frequency applications.

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