N-Face GaN-Based Microwave Metal-Insulator-Semiconductor High Electron Mobility Transistors by Plasma-Assisted Molecular Beam Epitaxy

Man Hoi Wong*, Yi Pei, David Brown, James S. Speck, and Umesh K. Mishra
ECE and Materials Departments, University of California, Santa Barbara, CA 93106-9560, USA
*Email: mhwong@ece.ucsb.edu; Tel: +1-805-893-5936
Michael L. Schuette, Hyeongnam Kim, Venkatesh Balasubramanian, and Wu Lu
ECE Department, Ohio State University, Columbus, OH 43210, USA

Keywords: GaN, N-face, AlN, molecular beam epitaxy (MBE), high electron mobility transistor (HEMT), microwave power

Abstract

This work investigates the use of N-face GaN-based heterostructures as a promising approach to overcome performance limitations commonly encountered in Ga-face AlGaN/GaN HEMTs as their frequency of operation extends into the millimeter-wave and beyond. N-face $(000\bar{1})$ GaN, with its reversed direction of polarization compared to that of the Ga-face (0001), are well-suited for designing new device structures that address the problems of poor electron confinement and high ohmic contact resistance in highly-scaled GaN transistors. The fabrication and characterization of two N-face MIS-HEMT structures by plasma-assisted MBE are presented. The devices demonstrated good RF performance at 4 GHz, with the highest continuous-wave output power density and power-added efficiency exceeding 8 W/mm and 70%, respectively. At 10 GHz, an output power density and power-added efficiency of 4.2 W/mm and 49%, respectively, were achieved.

INTRODUCTION

Since the report of the first GaN-based HEMT [1], much effort has been devoted to establishing the high frequency performance of AlGaN/GaN HEMTs from the S-band to the Ka-band and beyond. The high breakdown field of GaN and its alloys with Al allows AlGaN/GaN HEMTs to operate at much higher voltages than GaAs- or InP-based transistors. Due to the strong spontaneous and piezoelectric polarizations in AlGaN/GaN HEMTs, 2DEG channels with a very high charge density (in excess of 10^{13} cm^{-2}) can accumulate at the AlGaN/GaN interface. The atomic periodicity of the polarization charges ensures high 2DEG mobilities. These qualities, together with the high electron velocity in GaN, make AlGaN/GaN HEMTs an attractive candidate for millimeter-wave solid state power sources.

Even though numerous technologies have been developed to optimize the high frequency power performance of AlGaN/GaN HEMTs, these transistors have fallen short of delivering the expected capabilities for frequencies at the Ka-band and beyond (Fig. 1). While difficulties in high frequency device characterization such as non-optimal load-matching have contributed to an apparent degradation in performance, breakthroughs have also been hindered by the epitaxial structure. As the gate length of the devices decreases to allow for higher frequency of operation, increased confinement of the 2DEG becomes important for maintaining the modulation efficiency of the gate in order to reduce short channel effects. Techniques using double heterostructures, such as wide-bandgap buffers [2] and InGaN back barriers [3] were commonly employed to reduce current injection into the buffer by raising the conduction band edge in the buffer with respect to the channel. These techniques often reduce the rate of heat dissipation from the channel due to the low thermal conductivity of thick AlGaN buffer layers [2, 4], or introduce difficulties in material growth [3]. In addition, parasitic resistances limit the speed of the highly-scaled HEMTs, and reduce the gain and efficiency of the amplifiers. In Ga-face AlGaN/GaN HEMTs, the wide bandgap AlGaN barrier layer and its associated conduction band discontinuities with GaN have presented difficulties to realizing low contact resistances.

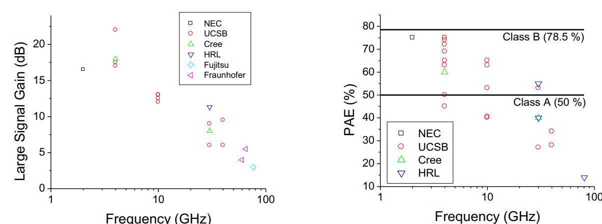

Figure 1. Maximum large signal gain (measured in the power sweep with the highest output power density) and maximum PAE of devices reported by different research groups vs. frequency of operation, showing a steady decrease in gain and PAE as frequency increases.

An alternative approach to overcome the aforementioned challenges encountered as device dimensions decrease is by growing HEMT structures inverted on the N-face $(000\bar{1})$ orientation (Fig 2). N-face GaN offers a few unique advantages for highly-scaled GaN-based transistors. Due to the absence of inversion symmetry in wurtzite (Ga,Al,In)N, the polarization in N-face materials is opposite to that in III-face (0001) materials. This enables N-face heterostructures where the 2DEG forms above the wide bandgap layer that

acts as an inherent back-barrier. The strong polarization-induced dipole moment of an N-face Al(Ga)N back-barrier strained to a GaN buffer enables the use of a thin Al(Ga)N layer to achieve a strong confinement potential with insignificant thermal resistance [4]. At the same time, the metal-to-2DEG connection in N-face devices does not need to go through a wide bandgap AlGaN layer, offering the potential of achieving much lower ohmic contact resistances in N-face devices [5]. Although early researchers have suggested the inferior quality of N-face heterostructures [6, 7], advances in growth on SiC substrates have enabled the development of devices based on N-face materials [8, 9]. Extensive developments of the growth and processing of N-face HEMTs have led to high room temperature 2DEG mobilities exceeding 1700 cm^2/Vs, and the successful demonstration of RF performance in these devices [10, 11].

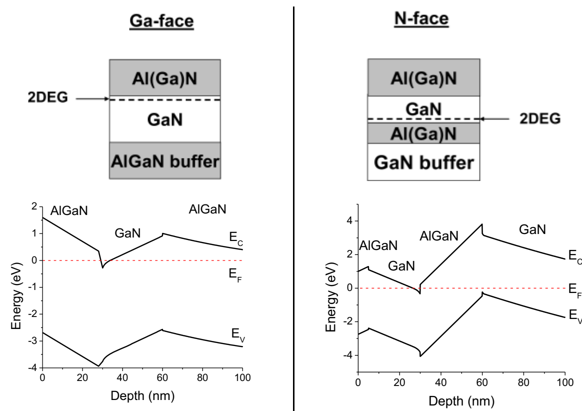

Figure 2. (Left) A thick AlGaN buffer used in a Ga-face AlGaN/GaN/AlGaN double-heterostructure. (Right) A thin AlGaN back-barrier used in a typical N-face transistor structure.

DEVICE DESIGN, GROWTH, AND FABRICATION

The simplest realization of an N-face HEMT is literally a Ga-face AlGaN/GaN HEMT turned upside down (Fig. 2). A GaN buffer is used instead of AlGaN due to the higher thermal conductivity of GaN [4]. Moreover, the strained AlGaN barrier generates piezoelectric polarization that adds to its spontaneous polarization to enhance the confinement potential and 2DEG density. An N-face GaN/AlGaN/GaN heterostructure can be capped by AlGaN to provide a larger Schottky barrier than with GaN, as well as a reversed polarization field under the gate for leakage reduction. The higher thermal stability of AlGaN alloys compared to that of GaN makes the former suitable as a surface protection layer for high temperature processing, such as high temperature deposition of dielectrics as insulators.

Fig. 3 shows an undoped N-face HEMT (E_C', E_V', E_F') consisting of $Al_{0.1}Ga_{0.9}N$ (cap)/ GaN (channel)/ $Al_{0.25}GaN_{0.75}N$ (barrier)/ GaN (buffer). The large dipole moment in the strained $Al_{0.25}Ga_{0.75}N$ enables the formation of a 2DEG at its top interface with GaN through the ionization of donor-like trap states (E_T') at 60 meV from the valence band edge at the opposite interface [12]. These states do not respond at high frequencies and their charging/discharging during transistor operation leads to dc-RF dispersion [10, 12]. To form a baseline N-face device (E_C, E_V, E_F), Si doping is added below the $Al_{0.25}Ga_{0.75}N$ barrier to supply charges to the 2DEG and satisfy the requirement for positive charges in the system. The ionization and modulation of trap states is prevented.

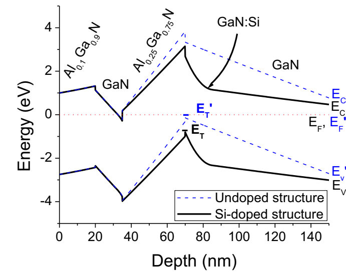

Figure 3. Band diagrams of an undoped and a Si-doped N-face HEMT. The Si-doping prevents the donor-like trap state (E_T) from being modulated by the Fermi level during transistor operation.

Electrons confined at the GaN/AlGaN interface experience strong alloy scattering from the AlGaN. A modified HEMT structure was therefore adopted where the 2DEG was confined at a GaN/AlN interface. The epitaxial structure and simulated band diagram of an N-face MIS-HEMT with an AlN back-barrier [13, 14] is shown in Fig. 4.

The devices were grown on 6*H*-SiC substrates in a Varian Gen-II PAMBE system. The growth temperature was 710-720 °C unless indicated otherwise. Initiating the growth with an N-rich AlN nucleation layer grown at 760 °C led to low impurity incorporation from the substrate into the buffer and hence reliable insulating buffers. A 0.6-µm thick two-step GaN buffer was used to reduce the threading dislocation density [9]. The two-step GaN-buffer approach, as well as higher AlN growth temperatures and thicker GaN buffers, effectively improved the twist mosaic of the GaN buffer with insignificant impact on the tilt mosaic [14]. A silicon δ-doping of 1.35×10^{13} cm^{-2} (implemented as 45Å-thick GaN with 3×10^{19} cm^{-3} doping) was used to supply charges to the channel and prevent modulation of slow-responding donor-like states near the valence band edge at the bottom AlN/GaN interface [10, 12]. A 3-nm AlN barrier layer induced a 2DEG at the top GaN/AlN interface, above which a 25-nm GaN channel layer was grown. The large conduction band discontinuity of GaN with AlN (ΔE_C), combined with the large dipole moment (ΔE_P) of AlN strained to GaN due to the large polarization coefficients of AlN, enable the use of only thin layers of AlN to achieve large 2DEG confinement potentials. For a 3-nm-thick AlN layer, the Schrödinger-Poisson simulation estimated a confinement potential to be larger than the bandgap energy of GaN. The electrons were further separated from the dopants by a 4-nm GaN-spacer layer to reduce remote ionized impurity scattering. The devices were capped by 5 nm of $Al_{0.1}Ga_{0.9}N$, which prevented surface degradation

during the subsequent deposition of a 5-nm-thick Si_xN_y gate insulator using HTCVD at 1020 °C. A thin cap layer with a low Al content of 10% was chosen to minimize depletion of the 2DEG due to its reverse polarization field.

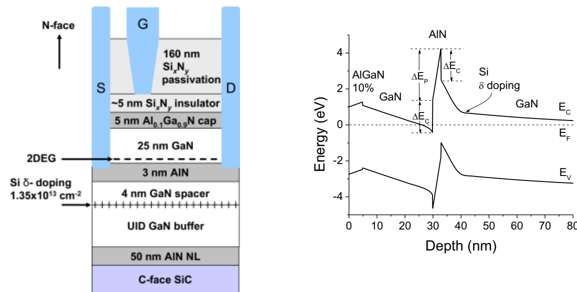

Figure 4. Epitaxial structure and band diagram of the N-face AlN back-barrier HEMT.

The back-barrier is an important degree of freedom for tailoring the 2DEG density in N-face HEMTs via polarization engineering, especially in scaled devices with a small gate-to-channel spacing where the depletion of the 2DEG due to the surface Schottky barrier becomes more severe. The electrostatic potential can be designed from behind the 2DEG using ionized dopants or judicious arrangement of dipoles generated by polarization charges. In the device described above, the 2DEG density can be increased with higher Si δ-doping density (1.35×10^{13} cm^{-2} → 1.65×10^{13} cm^{-2}, implemented as 55Å-thick GaN with 3×10^{19} cm^{-3} doping). To prevent the formation of a parallel channel due to the enhanced doping, a thicker AlN layer (3 nm → 5 nm) is used to increase the electric field at the δ-doping and eliminate parasitic conduction. However, the resultant steeper band profile below the AlN also brings the trap level (E_{T1}) at the AlN/GaN-spacer interface close to E_F at equilibrium. We therefore focus on a design in which the GaN-spacer is placed in between two AlN layers (AlN_1 and AlN_2) with the combined thickness of the two AlN layers (2 nm + 3 nm) being equal to that of the single thick AlN layer (5 nm) such that the total dipole moment due to the AlN remains the same (Fig. 5). Improved dispersion control is achieved since the polarization field in the GaN-spacer has been counteracted by an opposite field in the bottom AlN layer (AlN_2) before E_{T1} reaches E_F. This dual-AlN back-barrier scheme [15] has an added advantage of having both AlN layers below the critical thickness for cracking.

The devices were fabricated using alloyed Ti/Al/Ni/Au metal stacks as ohmic contacts. The Si_xN_y and $Al_{0.1}Ga_{0.9}N$ in the contact areas were removed by CF_4 and Cl_2 plasma, respectively, prior to metal evaporation to facilitate ohmic contact formation. Mesas were formed with BCl_3/Cl_2 reactive ion etch. The surface was subsequently passivated with Si_xN_y by PECVD. A timed etch using CF_4/O_2 plasma was used to remove the PECVD Si_xN_y under the gate and create a slanted sidewall profile [16], while keeping the HTCVD Si_xN_y as the gate insulator. Ni/Au/Ni (30/250/50 nm) was used as the gate metallization. Passivating the device prior to gate deposition ensured uniform Si_xN_y coverage at the edge of the gate metal. The nominal gate length was 0.7 μm and the gate-source spacing was 0.5 μm.

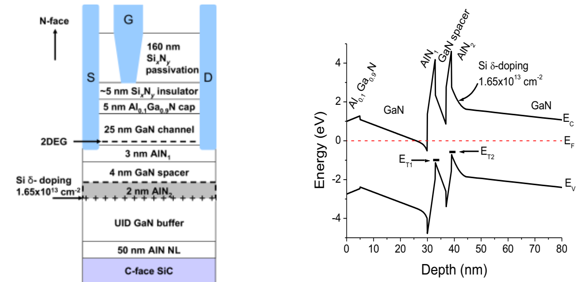

Figure 5. Epitaxial structure and band diagram of the N-face dual-AlN back-barrier HEMT. The schematic shows the placement of the second AlN layer (AlN_2) relative to the structure shown in Fig. 4 as a net result of the design procedure.

RESULTS AND DISCUSSION

I. AlN Back-Barrier MIS-HEMT

Room temperature Van der Pauw Hall measurements indicated a 2DEG density and mobility of 7.7×10^{12} cm^{-2} and 1350 cm^2/Vs, respectively. The maximum drain current I_{max} was 0.8 A/mm at V_G = +2 V. The buffer breakdown at 1 mA/mm, measured between the source and drain of a transistor with the channel etched away, was in excess of 160 V. The two-terminal gate-drain breakdown voltage at 1 mA/mm was 48 V.

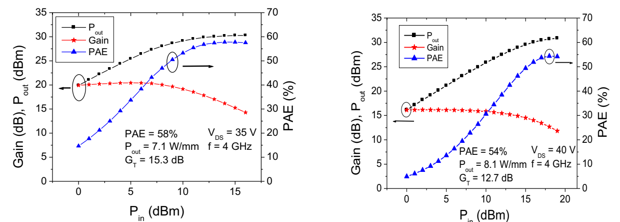

Figure 6. Large signal performance of the AlN back-barrier HEMT at 4 GHz with a drain bias of (left) 35 V and (right) 40 V. A highest P_{out} of 8.1 W/mm was achieved.

In devices with a gate width of 2×75 μm, small signal high frequency characterization was performed using an Agilent E8361A network analyzer. An f_T of 17 GHz and f_{max} of 37 GHz were obtained at I_{DS} = 520 mA/mm and V_{DS} = 25 V. Uncooled CW power measurements were performed using a Maury microwave load-pull system. Biased in deep class AB, measurements at 4 GHz with V_{DS} = 35 V and a quiescent drain current density of 100 mA/mm yielded a transducer gain (G_T) of 15.3 dB and an output power density (P_{out}) of 7.1 W/mm with an associated PAE of 58% (Fig. 6). The maximum linear gain was 20 dB in this device. On a separate device, a drain bias of 40 V and a quiescent drain current of 110 mA/mm yielded a G_T of 12.7 dB and a high P_{out} of 8.1 W/mm with an associated PAE of 54% (Fig. 6).

II. Dual-AlN Back-Barrier MIS-HEMT

Room temperature Van der Pauw Hall measurements revealed a 2DEG density and mobility of 1.1×10^{13} cm^{-2} and 1400 cm^2/Vs, respectively. This sheet resistance of 400 Ω/sq was a 33% improvement from the single-AlN back-barrier structure. Capacitance-voltage measurements confirmed the absence of parasitic channels. The maximum drain current I_{max} was beyond 1 A/mm at V_G = +2 V. A peak DC extrinsic transconductance ($g_{m,ext}$) of 200 mS/mm was achieved.

In devices with a gate width of 2×50 µm, an f_T of 17 GHz and an f_{max} of 58 GHz were measured at I_{DS} = 460 mA/mm and V_{DS} = 20 V. Biased in class AB, CW power measurements at 4 GHz with V_{DS} = 20 V and a quiescent drain current of 70 mA/mm yielded a G_T of 13.1 dB and a P_{out} of 4.1 W/mm with a high PAE of 71% (Fig. 7). At 28-V drain bias and a quiescent current of 65 mA/mm, a highest PAE of 67% was achieved with a P_{out} of 6.4 W/mm and a G_T of 13.1 dB (Fig. 7). This performance is comparable to Ga-face HEMTs with a similar gate structure. At 10 GHz, a PAE of 49% (drain efficiency = 57%) and a P_{out} of 4.2 W/mm were measured at V_{DS} = 20 V and a quiescent current of 46 mA/mm, with an associated G_T of 8.3 dB (Fig. 8).

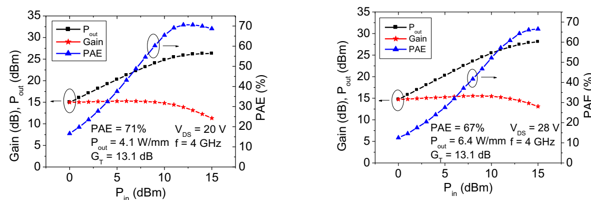

Figure 7. Large signal performance of the dual-AlN back-barrier HEMT at 4 GHz with a drain bias of (left) 20 V and (right) 28 V. A highest PAE of 71% was achieved.

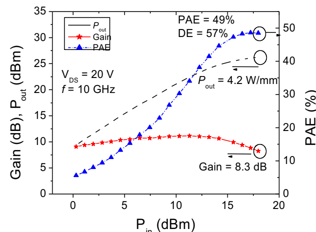

Figure 8. Large signal performance of the dual-AlN back-barrier HEMT at 10 GHz with a drain bias of 20 V.

CONCLUSIONS

The development of MBE-grown N-face MIS-HEMTs has led to their good large signal performance in the C- and X-bands. This work demonstrates that N-face devices can be used to generate microwave power, and represent an important step in engineering scaled N-face transistors.

ACKNOWLEDGEMENTS

The authors acknowledge funding support by the ONR MINE project (Dr. P. Maki and Dr. H. Dietrich). A portion of this work was done in the UCSB Nanofabrication Facility, part of the NSF-funded NNIN network. The band diagrams shown were generated by a 1D Schrödinger-Poisson solver *BandEng* [17].

REFERENCES

[1] M. A. Khan, A. Bhattarai, J. N. Kuznia, and D. T. Olson, *Appl. Phys. Lett.* **63**, 1214 (1993).

[2] M. Micovic *et al.*, "GaN Double Heterojunction Field Effect Transistor For Microwave and Millimeterwave Power Applications," in *IEDM Tech. Dig.*, 2004, pp. 807-810.

[3] T. Palacios, A. Chakraborty, S. Heikman, S. Keller, S. P. DenBaars, and U. K. Mishra, *IEEE Electron Device Lett.* **27**, 13-15 (2006).

[4] W. L. Liu and A. A. Balandin, *J. Appl. Phys.* **97**, 073710 (2005).

[5] M. H. Wong, Y. Pei, T. Palacios, L. Shen, A. Chakraborty, L. S. McCarthy, S. Keller, S. P. DenBaars, J. S. Speck, and U. K. Mishra, *Appl. Phys. Lett.* **91**, 232103 (2007).

[6] M. J. Murphy, K. Chu, H. Wu, W. Yeo, W. J. Schaff, O. Ambacher, J. Smart, J. R. Shealy, and L. F. Eastman, *J. Vac. Sci. Technol. B.* **17**, 1252-1254 (1999).

[7] R. Dimitrov, M. Murphy, J. Smart, W. Schaff, J. R. Shealy, L. F. Eastman, O. Ambacher, and M. Stutzmann, *J. Appl. Phys.* **87**, 3375 (2000).

[8] E. Monroy, E. Sarigiannidou, F. Fossard, N. Gogneau, E. Bellet-Amalric, J.-L. Rouvière, S. Monnoye, H. Mank, and B. Daudin, *Appl. Phys. Lett.* **84**, 3684 (2004).

[9] S. Rajan, M. Wong, Y. Fu, F. Wu, J. S. Speck, and U. K. Mishra, *Jpn. J. Appl. Phys.*, *Part 2* **44**, L1478 (2005).

[10] S. Rajan, A. Chini, M. H. Wong, J. S. Speck, and U. K. Mishra, *J. Appl. Phys.* **102**, 044501 (2007).

[11] M. H. Wong, S. Rajan, R. M. Chu, T. Palacios, C. S. Suh, L. S. McCarthy, S. Keller, J. S. Speck, and U. K. Mishra, *Phys. Status Solidi A* **204**, 2049 (2007).

[12] A. Chini *et al.*, "An Experimental Method to Identify Bulk and Surface Traps in GaN HEMTs," 32nd Int. Symp. Compound Semiconductors, Rust, Germany, Sep. 18-22, 2005.

[13] M. H. Wong, Y. Pei, R. Chu, S. Rajan, B. L. Swenson, D. F. Brown, S. Keller, S. P. DenBaaras, J. S. Speck, and U. K. Mishra, *IEEE Electron Device Lett.* **29**, 1101 (2008).

[14] M. H. Wong, Y. Pei, J. S. Speck, and U. K. Mishra, *Appl. Phys. Lett.* **94**, 182103 (2009).

[15] M. H. Wong, Y. Pei, D. F. Brown, S. Keller, J. S. Speck, and U. K. Mishra, *IEEE Electron Device Lett.* **30**, 802 (2009).

[16] Y. Dora, A. Chakraborty, L. McCarthy, S. Keller, S. P. DenBaars, and U. K. Mishra, *IEEE Electron Device Lett.* **27**, 713 (2006).

[17] Available: http://my.ece.ucsb.edu/mgrundmann/bandeng

ACRONYMS

CW: Continuous Wave
HEMT: High Electron Mobility Transistor
HTCVD: High Temperature Chemical Vapor Deposition
MIS: Metal-Insulator-Semiconductor
PAE: Power-Added Efficiency
PAMBE: Plasma-Assisted Molecular Beam Epitaxy
PECVD: Plasma-Enhanced Chemical Vapor Deposition
RF: Radio Frequency
2DEG: 2-Dimensional Electron Gas