Demonstration of Enhancement Mode AlN/ultrathin AlGaN/GaN HEMTs Using A Selective Wet Etch Approach

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Abstract

A novel recessed-gate structure involving an ultrathin AlGaN barrier layer capped by an AlN layer in the source-drain access regions has been implemented to demonstrate enhancement-mode high electron mobility transistors. A wet etch process has been developed using heated photoresist developer to selectively etch the AlN for the gate recess step, bypassing plasma etching and associated issues. The etch has been proven to be selective to AlN over AlGaN and GaN. A repeatable threshold voltage of +0.21V has been demonstrated with 4 nm AlGaN barrier layer thickness.

INTRODUCTION

Modern applications require ever more powerful and more efficient power delivery systems. The AlGaN/GaN High Electron Mobility Transistor (HEMT) has attracted considerable attention as a candidate next-generation device for both microwave and high power switching applications. The material system has demonstrated excellent thermal and chemical stability, as well as high mobility and breakdown field. [1-5] A long sought goal though has been the development of a reliable, fast, efficient, normally-off power switch. Such a device would have a wide range of immediate military power converter applications, such as high-power satellite communications and radar, unmanned underwater vehicles, ship drive components, and hybrid vehicle inverters.

Most progress toward enhancement mode AlGaN/GaN HEMTs has focused on plasma-based methods such as gate recess etching [6-8] or fluorine ion implantation to turn off the channel under the gate. [9-11] However, a wet etch approach is desirable from a manufacturing perspective since it offers more reliability since an etch stop structure can be implemented. This is a follow-up to initial work demonstrating the development of enhancement mode AlGaN/GaN HEMTs using such a wet etch approach [12]. The structure consists of an AlGaN/GaN HEMT with an ultrathin AlGaN barrier layer for positive threshold voltage, then an AlN capping layer to reintroduce strain, and thus 2DEG carriers. The AlN layer can be selectively wet etched in the gate region to turn off the channel under the gate. A schematic of this structure is shown in Figure 1. Wet etching

of AlN using heated AZ400K photoresist developer has been previously reported [3,13], but etch selectivity to AlGaN has not been investigated.
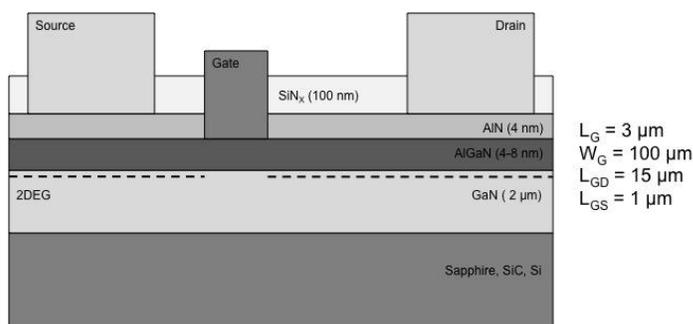

Figure 1. Cross section of AlN/ultrathinAlGaN/GaN HEMT

MATERIAL GROWTH & CHARACTERIZATION

Three HEMT structures were grown on a-plane Al_2O_3 substrates by MOCVD. The first structure was 25 nm AlGaN/2 um undoped GaN on an AlN buffer layer as a reference HEMT. The wet etch test structures included an initial 2μm undoped GaN layer on an AlN nucleation layer, followed by either 8 or 4 nm $Al_{0.3}Ga_{0.7}N$ layers, followed by 4 nm AlN cap layer grown at 1050 °C. The sheet resistance for all samples was ~1100 Ω/sq, measured with a Lehighton probe and confirmed by TLM. The sheet carrier concentration was ~6×10^{12} cm^{-2} with a mobility of ~ 1000 cm^2/V-s at room temperature for all samples, determined by Hall measurements. Mesas were formed using an Inductively Coupled Plasma etch with Cl_2/Ar chemistry. Ohmic contacts were then deposited by lift-off of e-beam evaporated Ti/Al/Ni/Au, followed by an RTA at 900 °C for 30s in flowing N_2 atmosphere. The resulting contact resistance was $2x10^{-6}$ Ω-cm^2. To form a passivation layer and hard mask for the gate opening etch, PECVD SiN_X was deposited and subsequently patterned using a SF_6-based RIE etch, also opening the ohmic contacts. The gate opening process on the wet etch test structures implemented selective chemical etching of the AlN using AZ400K developer at 85 °C. The gate was then formed by lift-off of e-beam evaporated Ni/Au.

In order to confirm the linear relationship between threshold voltage and AlGaN thickness, simulations were

performed using a 1-D Poisson solver. C-V profiles were simulated over a range of AlGaN thickness, and V_T was extracted. To investigate experimentally, the reference HEMT was split and a gate recess etch was performed using a low power Cl_2/Ar ICP for varying times up to 90s, corresponding to a remaining AlGaN thickness of <2 nm. C-V profiles were measured, and the threshold voltage and AlGaN thickness (assumed to be the depletion layer thickness) were extracted. The experimental values matched extremely well with the simulated values, as shown in Figure 2. Based on this line, the AlGaN thickness for the wet etch structure was chosen to be 4 nm to correspond with a positive V_T.
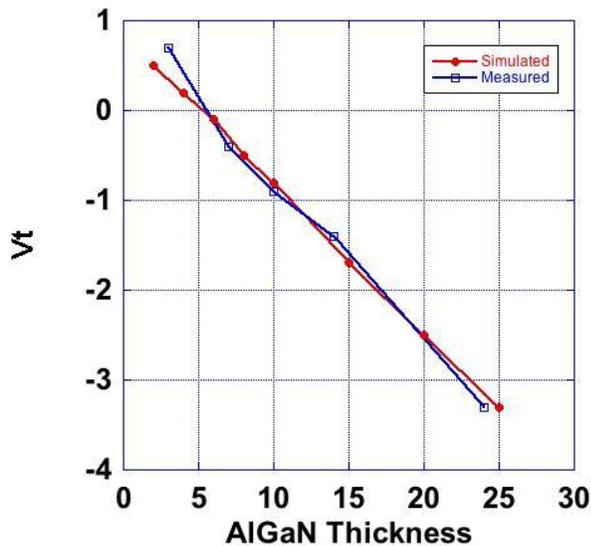

Figure 2. Simulated and measured Vt from C-V profiles. Measured AlGaN thickness is also extracted from C-V.

WET ETCH RESULTS

To test etch selectivity, the wafer with 4 nm AlN/8 nm AlGaN/2 μm GaN was diced into 8 pieces and etched with durations from 0-70 minutes in 10 min intervals. It is clear from scanning electron microscopy (SEM) on ungated samples (not shown) that the gate recess dimension becomes larger after 20 min etching compared to the as-patterned feature in the hard mask. This implies that the etch mechanism is isotropic, as it etched laterally in the source-drain region and visibly undercut the SiNx mask for the very long etch times. The open gated current was measured before and after etching. Further characterization using X-ray photoelectron spectroscopy (XPS) has confirmed the selectivity of the etch.

After depositing gates on the devices from the 4 nm AlN/8 nm AlGaN/2 μm GaN wafer, the FET I-V curves were measured and the threshold voltage was extracted as a function of etch time, shown in Figure 2. After an initial shift from -1.3V to -0.4V after 10 minutes etching, V_T remained constant for the range of etch times studied. The constant threshold voltage implies that the AlGaN barrier is

intact, and the thickness does not change with etch time. Also shown in Figure 2 is the on-resistance of the devices, which increases initially, due to the high-resistance region under the gate being formed when the channel becomes depleted, then remaining constant up to 20 min, then further increasing as the lateral etch broadens the feature and increases the resistance in the access regions. This clearly supports the etch stop hypothesis. The current level continues to degrade with etch time as the AlN is laterally etched, thus decreasing polarization and increasing the resistance in the access regions.
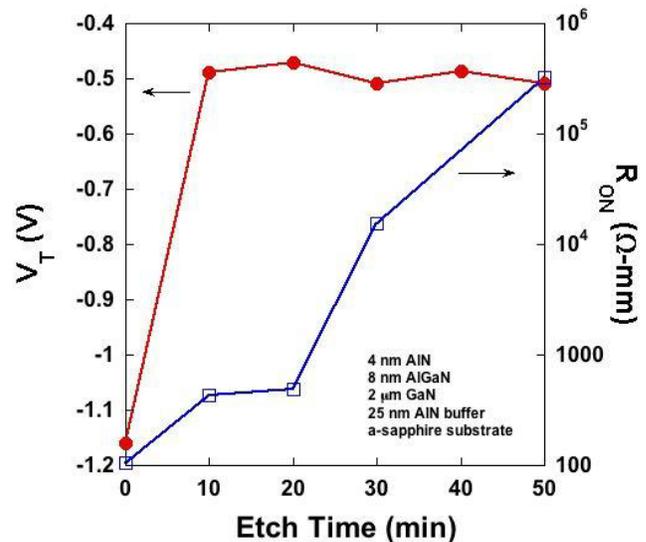

Figure 3. Threshold voltage and on-resistance for 4 nm AlN/8 nm AlGaN/2 μm GaN structure

Based on the initial positive results, a wafer was grown with a 4 nm thick AlGaN layer, which was expected to yield a positive threshold voltage based on fundamental calculations and the simulations and data in Figure 2. described below. Fabrication was completed as described previously. From the FET I-V curves, shown in Figures 3 and 4, a threshold voltage of +0.21 V was extracted. This value was reproducible within 0.02V across the entire quarter wafer that was processed. The saturation current was 41 mA/mm at Vg = 2.5V and the maximum transconductance was 33 mS/mm at Vg = 0.5V. While current density was low due to the relatively high sheet resistance and large gate length (3-5 μm) and gate-drain gap (15-20 μm), it is comparable to that found in an unetched structure with similar sheet resistance. The mesa-to-mesa isolation current was 0.2 mA at 10V, which implies that off-state current is limited by buffer leakage for this particular sample.
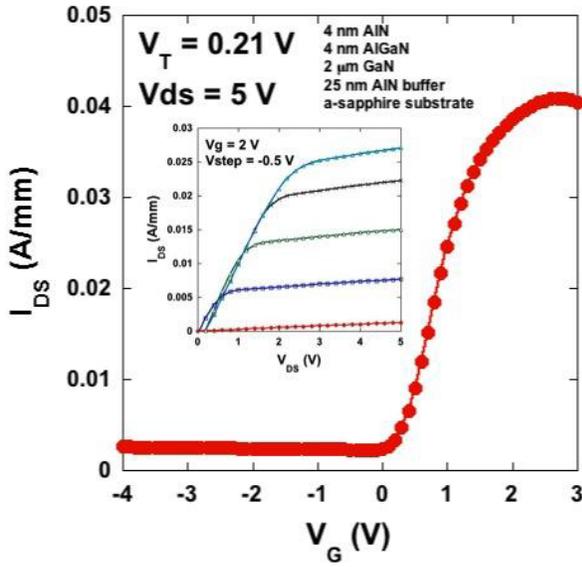
Figure 4. V_{GS}-I_{DS} curve for 4 nm AlN/4 nm AlGaN/2 μm GaN. V_{DS}-I_{DS} curve is shown as inset

FUNDAMENTAL CALCULATIONS

Saito, et al. has detailed both theoretically and experimentally a linear relationship between threshold voltage and recessed AlGaN thickness using low power ICP etching with the following equations. [8]

$$V_T = \phi_B + \frac{qN_{2D}}{\varepsilon}\left(t_{CR,G} - d\right)$$

$$t_{CR,G} = \frac{\left(\Phi_B - \Delta E_C\right)\varepsilon}{qN_{2D}}$$

In these equations, Φ_B represents the Schottky Barrier Height, N_{2D} represents the 2DEG density, d represents the recessed AlGaN thickness, and ΔE_C represents the conduction band offset. Using an interpolated value for ΔE_C from the literature [14], the actual 2DEG density from Hall measurements, and the barrier height extracted from source-gate I-V characteristics, the threshold voltage is accurately predicted for both the 4 and 8 nm AlGaN cases. Furthermore, this value is consistent with reports of structures using comparable AlGaN thickness. [15]

Further investigation of this structure using the 1-D Poisson solver mentioned above has led to some interesting observations about this structure. The band diagram, shown in Figure 5, seems to indicate the presence of two 2DEG channels – one at the AlN/AlGaN interface and one at the AlGaN/GaN interface. While this may be positive from a saturation current and breakdown voltage perspective, it may be a source of leakage if the AlN layer is not completely cleared by the wet etch. Therefore further work is necessary to completely understand the etch mechanism and determine the precise etch rate.
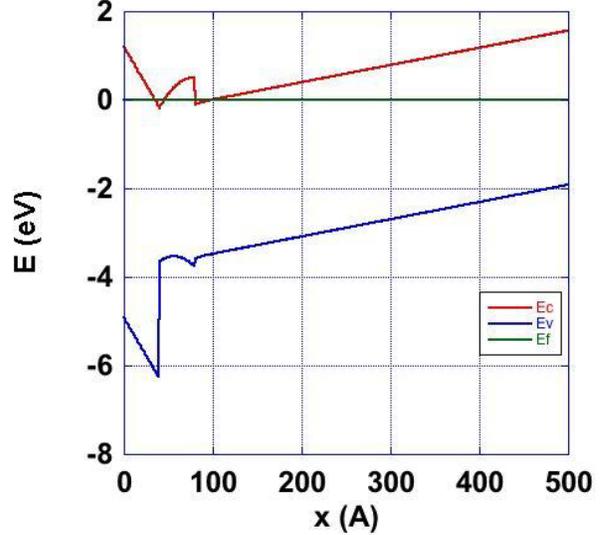

Figure 5. Simulated band diagram of 4 nm AlN/4 nm AlGaN/2 um GaN structure

CONCLUSIONS

In conclusion, a device structure has been demonstrated incorporating an ultrathin AlGaN barrier for accurate and reliable threshold voltage control, capped with a thin AlN layer in the source-drain access region to maintain high 2DEG charge. A fabrication process for this structure has been demonstrated which implements a selective wet etch of the AlN using heated photoresist developer for the gate opening step, thus bypassing plasma etching. This process has been employed using a 8 nm and 4 nm AlGaN barrier to demonstrate HEMTs with a threshold voltage of -0.48 and +0.21V, respectively, while maintaining a high mobility (>700 cm^2/V-s) and with little loss in current density relative to an unetched device.

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ACRONYMS

HEMT: High Electron Mobility Transistor
MOCVD: Metal Organic Chemical Vapor Deposition