GaN on Si Based Power Devices: An Opportunity to Significantly Impact Global Energy Consumption

Michael A. Briere

ACOO Enterprises LLC, Woonsocket RI USA, acompanyofone@aol.com, 310-529-2023

KEYWORDS: GaN on Si HEMT, ENERGY EFFICIENCY, COMMERCIALIZATION

ABSTRACT

A summary is presented of opportunities to significantly impact global energy consumption, by more than 25 % in 2025, through the use of more efficient working load architectures, enabled by new power electronics, provided that significant and rapid adoption of these architectures occurs. The rate of adoption is determined, to a large extent by the economic barriers or incentives involved. The availability of new power electronics based on commercially viable wide band gap semiconductors such as GaN on silicon power devices fabricated in silicon foundries, provides the required performance to cost value proposition to enable lower economic barrier to adoption for these energy efficient architectures. Evidence for the commercially viable manufacturabity of these devices will be presented.

INTRODUCTION

It is well established that due to increases in standard of living throughout the world, total energy consumption is expected to increase by at least 35 % over the next 20 years [1].

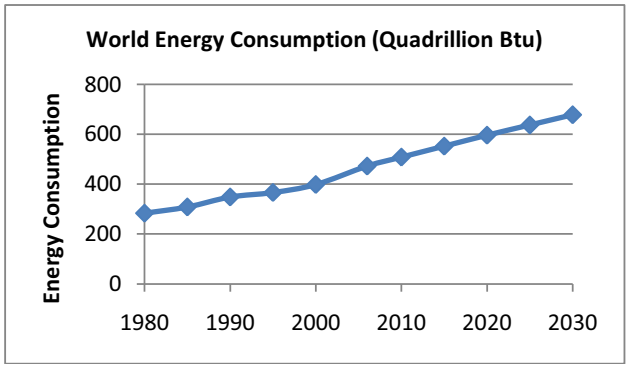

Fig. 1: World Marketed Energy Consumption [1]

It is less well known that a significant reduction in worldwide energy consumption can be achieved through the wide spread adoption of improved load architectures [2,3]. These include the use of electric motors, in replacement of, or in conjunction with smaller, internal combustion engines potentially saving 60% of the nearly 20% of all energy that is consumed through transportation. Improving efficiency of motion control, including the replacement of ac induction motors with inverter driven permanent magnet motors in consumer appliances represents another substantial opportunity, saving over 50 % of the 50% of all electricity, 20 % of all energy consumption, used for motor drive applications. In addition, the replacement of incandescent light bulbs with electronic ballasted compact fluorescent or light emitting diode based lighting can save nearly 75% of the 20% of electricity, 8 % of total energy consumption used by lighting. Further, improved energy efficiency and distributed architectures in delivering power for electronic loads, especially within the growing IT infrastructure, is an opportunity to save more than 20 % of the energy used in such applications, which today represents more than 15% of electricity usage and 6% of total worldwide energy consumption. In total, over 25 % of worldwide annual energy consumption can be saved through widespread (i.e. >90 %) adoption of these efficient load technologies enabled by advanced power electronics.

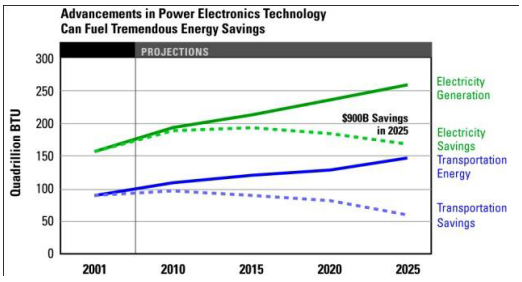

Figure 2: Potential Global Energy Savings based on Widespread Adoption of More Efficient Working Loads (cost savings assume $40/barrel)

The energy savings are, for the most part, achieved through the nature of the working load, though the performance of the

loads requires substantial, optimized and intelligent power electronics. Even though both the required loads and the necessary power electronic architectures are, in principle, presently available to implement these energy saving solutions, adoption is expected to remain relatively anemic for at least another decade. This is due to the price premium which is passed to the end consumer of the complete systems incorporating these energy efficient solutions. Only when this premium is substantially reduced or eliminated, will the adoption of energy efficient systems approach dominance, a necessary requirement for substantial worldwide energy savings. The reduction of total system costs can be substantially enabled by intelligent power electronics which optimize performance/cost.

POWER ELECTRONICS PERFORMANCE

Modern power electronics solutions provide an array of system level enhancements such as communication protocols, load condition reporting, as well as optimal balancing and coordination and protection of power conversion sub-systems and loads. As important as these advances have been, it is the continued progress in the performance of the power converter sub-systems themselves that have enabled increasingly dense and efficient working loads.

It can be argued that the intrinsic value proposition of the power conversion sub-systems is density*efficiency/cost. This performance/cost figure of merit (FOM) for power processing is the equivalent driving force behind innovation as the logic unit/ $ FOM is to the well known Moore's law of the data processing industry. There have been significant advancements in both FOMs over the past 40 years. It can be argued that the most significant advances in energy conversion efficiency* density/cost have been achieved through requisite improvements in the power devices used. Generally, advances through improved circuit architectures, from linear to switching regulation, hard to soft switching, passive to synchronous rectification, etc., have all been accomplished by leveraging the inherent capabilities and avoiding the inherent limitation of the power switch components used. It can therefore be expected that radically improved power switch performance might well drive a revolution in power electronic architectures and systems.

POWER DEVICE PERFORMANCE

The ability of power semiconductor devices to enhance the power electronics performance/cost figure of merit can be simplified by its own price/ performance figure of merit, namely switching power loss* ohmic power loss *cost, where the switching power loss reflects the thermal limitation of density, most often achieved through increasing switching frequency and subsequent reduction in output filter components. For inverter circuits this can be referred to by Qrr* Vceon*cost or more precisely Eoff* Vceon*cost, for silicon based IGBT switch/ diode pairs. For dc-dc converter circuits such as common buck regulators, the FOM is R(ds)on*Qsw*cost. Here the specific-on-resistance, R(on), times cost, also serves to represent the generic price / performance figure of merit of a power switch as $/Amp.

THE END OF SILICON DEVICE DOMINANCE

Since the advent of commercially viable silicon power FETs, introduced some 30 years ago, enabled the widespread adoption of switch-mode power supplies, replacing the linear regulator as the dominant power architecture, the silicon power FET has become the dominant power device. The silicon based IGBT, combining the ease of charge control with the benefits of conductivity modulated drift resistivity, has been another mainstay, especially in the lower frequency conversion systems, e.g. motor drive inverters. Of course, the same minority carrier injection that provides for lower ohmic losses also increases switching losses through the effects of subsequent tail currents. Over the last 3 decades significant engineering efforts have driven the improvement in the performance figure of merit of these silicon power devices by more than an order of magnitude. However, as this technology approaches maturity, it becomes increasingly expensive to achieve even modest improvements in the device FOM. It is estimated that less than a factor of two improvement will be economically feasible to achieve for 30 V FETs [4], with perhaps a factor of five possible for 600 – 1200 V silicon IGBTs [5]. If further advances in power device performance are required by future electronic loads, as is currently apparent, then these advances must be achieved through the use of alternative materials.

Necessary further advances in power device performance must be achieved through the use of alternative materials. One of the most promising alternatives to silicon is gallium nitride based power devices.

Even though the basic GaN HEMT transistor was first invented over 15 years ago by M. Asif Khan [6], significant development efforts on practical power devices using GaN-on-Si technology have been fairly recent, predominantly in the past 5-7 years. GaN based power devices are expected to improve rapidly over the next 10 to 20 years. In fact, it is expected that an order of magnitude in improvement in the key device performance FOMs will be achieved over the next 5 years.

In addition to efficiency improvements, the use of wide band gap semiconductors instead of state of the art silicon based devices for power electronic systems allows the reduction of size/weight of the conversion subsystems by between 2 and 10 fold, further promoting adoption.

BARRIERS TO COMMERCIALZATION

There have been however, several significant barriers to the commercialization of GaN based power devices. Chief amongst these is the cost of production. The production of power devices includes the costs of substrate, epitaxy, device fabrication, packaging, support electronics and development.

The viable economic based limit of about $ 3 / cm^2 for substrate and epitaxy cost set by the power device marketplace is exceeded by all substrate choices except silicon wafers. Multi-wafer MOCVD tools provide the required throughput and cost of ownership.

Next to the cost of substrate and epitaxial layers, device fabrication costs are the most critical. In fact, currently, substrate diameters of at least 150 mm are required to achieve widespread commercial viability for power device fabrication. It has been typical in compound semiconductor device fabrication to use specialized processes such as e-beam and lift-off lithography, as well as to utilize gold metallization. These techniques are understandable for military and RF applications, where markets will support costs of more than $ 10,000 for finished 100 mm wafers for discrete devices. The broad power device market will not support this order of magnitude fabrication costs. In fact, to gain broad adoption of alternative material based power devices, fabrication costs must approach that of silicon based power devices. In fact, the device fabrication costs are only acceptable if high volume, high yielding standard (silicon compatible) semiconductor fabrication lines are used. Similarly, the volume necessary to support the broad power device market (10 million 150 mm wafer equivalents per year) requires scalability in device manufacture provided most readily by existing silicon device fabrication facilities.

One example of a technology program that has been developed to address these issues is the GaNpowIR platform of International Rectifier [3]. This technology platform uses GaN-on Si hetero-epitaxy and device fabrication processing that can be performed in a standard modern silicon CMOS manufacturing line with little modification to equipment or process discipline. This allows this technology platform to provide power devices with compellingly superior performance/cost FOMs compared to silicon which will promote widespread adoption. The following provides evidence for the resolution of several barriers to commercialization of GaN based power devices.

BARRIERS OVERCOME

One of the most fundamental challenges to the commercialization of GaN based power devices is the development of cost effective, high yielding, high throughput III-Nitride epitaxial processes on large diameter silicon wafers. It is well established that silicon is the substrate of choice for commercial GaN based power devices. The intrinsic mismatch in both lattice constant and thermal coefficient of expansion with the requisite III-Nitride epitaxial films causes threading dislocations, as well as significant macroscopic film stresses, which result in excessive wafer bow and plastic deformation (cracks) in the films. These issues have been addressed by engineering the proprietary epitaxial film growth on standard thickness 150 mm (111) silicon wafers to both eliminate most of the threading dislocations, resulting in 10^9 cm^{-2}, predominately edge dislocations for 2 um thick films (comparable to similar thickness films grown on SiC), as well as compensating for the stresses due to thermal coefficient mismatches. These result in a high quality device layer, as demonstrated by the excellent electron Hall mobility of > 2000 cm^2/Vs achieved in the 2 dimensional electron gas formed at the interface between the thick GaN buffer layer and the overlying AlGaN barrier layer.

In addition, the resulting wafer bow of < 20 um (3 sigma), is well within the required limit for device fabrication of < 60 um. It should be noted that truly crack free material to within 0.5 mm of the wafer edge are consistently produced by this process in manufacturing volume

Much of the reported constructions for GaN devices to date utilize Schottky gates and subsequently exhibit device leakage in operation of mA/mm of gate width. For a power device, which often has an effective gate width on the order of 1 meter, such gate leakage would result in an unacceptable power loss/heating. Similarly, the maximum operating voltage has often been specified at reverse bias source-drain current densities of mA/mm of gate width. Another challenge, therefore, is the reduction of these leakage currents to less than 1 uA/mm. This has been achieved through the combined use of a proprietary insulated gate construction and improved III-Nitride epitaxial film quality. This has resulted in gate and drain-source leakages of < 10 pA/mm, as shown in Figure 3. The resulting ratio of Ion/Ioff of 10^{12} is substantially better than reported elsewhere for GaN based devices and even exceeds that of comparable silicon based power devices.

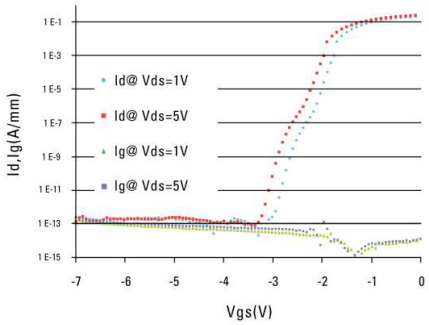

Figure 3: Measured Id , Ig normalized to gate width (850 mm) as a function of Vgs for Vd= 1 and 5 V, Lg=0.3 um.

Though the principle challenge to develop high voltage GaN on Si based devices which substantially exceed the performance of silicon based devices appears met to a large degree [e.g. 4,7,8], substantial challenges existed to produce low voltage devices to exceed silicon device performance. One such challenge is the reduction and control of source-drain contact resistance. Though this component to the Rdson of a high voltage device (e.g. > 300 V) is negligibly small, it can dominate the FOM for low voltage devices (e.g. < 100V). In fact, in order to be competitive, the contact resistance for low voltage devices must approach 1micro-ohmcm^2 or < 0.35 ohm mm. This has been achieved in a cost effective, high volume without the use of gold metallurgy, as shown in Figure 4.

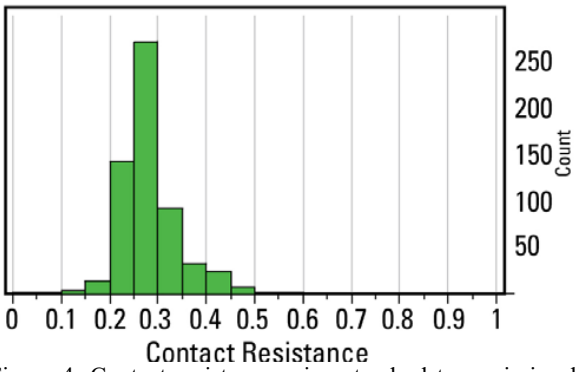

Figure 4: Contact resistance using standard transmission line technique for initial GaNpowIR platform

Another challenge for the realization of commercially viable low voltage GaN devices is the effective conduction of the source-drain current from the internal to the external device terminals. This has been accomplished through the use of planarized multi-level metallization, common to silicon ULSI device fabrication. In addition, the use of a proprietary solderable front metallurgy (SFM) has been used to produce a flip-chip die, eliminating wire bonding and minimizing other package related parasitics. Figure 5 shows such a flip chip GaN power device.

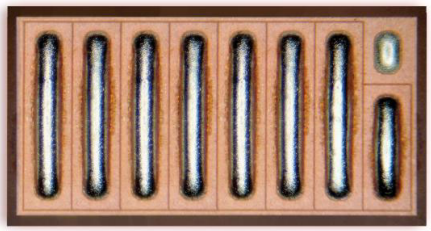
Figure 5: Topside view of a flip chip GaNpowIR device

Device yield is an important challenge for the commercialization of large area power devices. It is economically imperative that yields > 80 % are commonly achieved for large devices (e.g. > 15 mm^2). Figure 6 shows a wafer map of device yield for 15 mm^2 devices, demonstrating the necessary level of process maturity for commercialization.

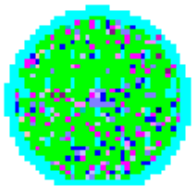
Figure 6: Wafer yield map for production GaNpowIR fabrication process for 15 mm^2 die.

It is interesting to note that much of the remaining yield loss is unrelated to the properties of the III-Nitride epitaxial layers.

Finally, the stability of device in-circuit performance is a prerequisite to commercialization. The critical FOM, Rdson shows excellent stability under accelerated conditions for > 4000 hrs. In fact, over 1,000,000 device hrs of reliability testing has shown performance in line with silicon based device specifications. Tests have included, gate stress, reverse bias stress, constant current (2x specification), temperature humidity bias, package testing for MSL and temperature cycling, high temperature operating life and intermittent operating life tests.

CONCLUSION

A great opportunity for the power electronics community is presented to significantly impact future global energy consumption, with its many sociological, environmental and economic consequences. It has been argued that a cost effective means of producing GaN based power devices will help achieve the necessary adoption rates to meet this challenge. International Rectifier's GaNpowIR platform is such a technology platform. Key barriers to commercialization, along with effective resolutions have been presented. It is expected that GaN on Si based power devices built on such platforms will enable rapid adoption of highly efficient working load systems and help to provide the desired energy conservation in the near future.

REFERENCES

[1] www.eia.doe.gov/iea
[2] Lidow, A., APEC 2005 Planery Talk and Briere, M.A., S2k Conference 2005
[3] M.A. Briere, Proceedings of PCIM Europe 2009 p. and Briere, M.A., Power Electronics Europe (7), October / November 2008 pp. 29-31
[4] Ikeda et.al. ISPSD 2008 p. 289
[5] Nakagawa, A., ISPSD 2006 p.1
[6] Khan, M.A. et.al, Appl. Phys. Lett (63) p.3470, 1993.
[7] S. Iwakami et.al. JJAP vol 46 (24) 2007 pp L587-L589
[8] Selvari et.al. IEEE EDL vol 30 (6) June 2006 p.588

ACRONYMS

FOM: Figure of Merit
HEMT: High Electron Mobility Transistor
FET: Field Effect Transistor
IGBT: Insulated Gate Bipolar Transistor
2DEG: Two Dimensional Electron Gas