# Design and Layout of Multi GHz Operation of Light Emitting Diodes

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**Keywords: LET, LED, modulation, GHz, spontaneous**

**Abstract**

**A new high-speed form of light emitting diode (LED) is demonstrated by utilizing an n-type buried "drain" layer beneath the p-type "base" quantum-well (carrier and photon) active region. The asymmetric two-junction LED employs the "drain" layer to tilt and pin the charge in the manner of a heterojunction bipolar light emitting transistor (HBLET), thus preserving the fast recombination lifetime in the order of carrier transit time in the thin base design ($\tau_B \sim \tau_t$) by removal of excess slow-recombining carriers in the base. A modified layout based on the tilted-charge LED characteristics is designed to further reduce the parasitics compared to conventional aperture design, and significantly enhance the spontaneous optical modulation bandwidth toward multi-GHz operation.**

## INTRODUCTION

Light emitting diodes (LEDs) can be a great potential candidate for shot-range data communication and interconnect due to their high yield, robustness, and low cost characteristics comparing to diode lasers. Many efforts have been explored to enhance the transmission speed of the LED from the initial kHz-MHz bandwidths to as much as 1.7 GHz [1]-[4]. For the past decade, the highest speed achieved by a spontaneous LED has been 1.7 GHz with the active layer doped $7x10^{19}$ $cm^{-3}$ to reduce the effective recombination lifetime to ~ 100 ps [4]. In our early work we employ a new class of light emitter, a three-port heterojunction bipolar light-emitting transistor (HBLET) [5] incorporating base quantum wells (QWs) to demonstrate both electrical and optical modulation at 1 GHz [6]. Due to the short base effect of tilted charge population in transistors, the effective minority carrier lifetime in the base region of the HBLETs can be progressively reduced to sub-100 ps by tailoring the doping and incorporating QW(s) [7]. The spontaneous optical modulation bandwidth of HBLETs can therefore be enhanced toward multi-GHz operation [8-9].

Recently we have proposed a new kind of LED, the "tilted-charge" LED, by incorporating a "drain" layer close to the QW-embedded p-doped active region to remove excess slow-recombination carriers, which results a high-speed optical operation as the HBLET [10]. Similar to the function of base-collector junction in the HBLET, the boundary condition at the base-"drain" junction results in a tilted base charge population. The injected minority carriers that recombine in the base form the base current, $I_B$, while carriers that are too "slow" to recombine within the transit time from the emitter to the collector-"drain", $\tau_t$, are removed by the base to drain junction reverse bias field (the "drain" current, $I_D$, Fig. 1). Therefore, the charge population in the base of the transistor can be modulated at intrinsic (parasitic-free) speeds corresponding to an effective recombination lifetime $\tau_B \sim \tau_t$. Assuming a tilted triangular population, we approximate $\tau_t$ as $W_B^2/2D$ where $W_B$ (Fig. 1) is the base width, or emitter-to-"drain" distance and $D$ is the diffusion constant. For a thin-base transistor where $W_B \sim$ 1000 Å, $\tau_t$ is typically on the order of several picoseconds. Taking into account the presence of parasitics due to finite non-zero junction capacitances and Ohmic losses, we expect $\tau_B$ in the sub-100 ps range. The possibility of "fast" picosecond recombination dynamics (induced with a tilted-charge base population) provides the basis for gigahertz modulation of the light emitting transistor [6-9], and now, the light emitting diode.

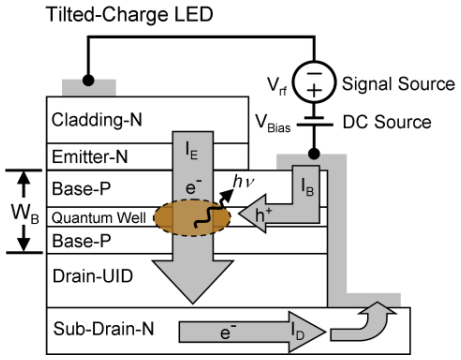


Fig.1 Schematic of tilted-charge LED

In the high speed modulation of an HBLET, the extrinsic parasitic capacitive charging delay due to lateral

extrinsic carrier transport effects ultimately limits the maximum optical bandwidth achievable and must therefore be taken into account. We have verified this by showing that the extrinsic-parasitic-limitations on the recombination lifetime can be reduced sufficiently to give $\tau_B < 100$ ps by laterally scaling the emitter aperture width from 13 μm to 5 μm to reduce the extrinsic capacitive charging and simultaneously increase the current density [9].

In this paper, we try to propose a new kind of layout design and reduce the parasitics (i.e. resistances and capacitances) from the conventional LED aperture layout by designing a new device configuration, lateral-feeding design, which is expected to improve the resistance issue faced when we try to scale the device using aperture layout.

## LAYOUT DESIGN

Conventionally, the layout design for surface-emitting devices (LEDs or vertical-cavity surface-emitting lasers (VCSELs) is a ring-contacted, oxide-confined aperture layout (Fig. 2a) in corporation with oxidation process first invented by Nick Holonyak Jr. in 1991 [11]. The oxide is used to confine the injected current flow and increase the radiative recombination uniformity. In the HBLET structures, due to the 'ring'-like geometry (Fig. 2a), the proper intrinsic base spans a concentric region with a radius ~ $D_A/2$, and an intrinsic device width $t$. Hence, the proportion of intrinsic base recombination to the total (extrinsic and intrinsic) recombination can be estimated with simple ratio, ~ $\pi D_A t/\pi(D_A/2)^2 = 4t/D_A$. As the device aperture width is reduced, increasingly larger proportion of the injected carriers are confined to the intrinsic base region (i.e., higher $4t/D_A$). Lateral extrinsic recombination therefore forms an equivalent parasitic-like RC-charging time that limits the optical bandwidth of the device.

The lateral extrinsic resistance R seen from this layout is proportional to the eq. (1).

$$R_{cir} = \frac{R_{sh}}{2\pi}\ln\left(\frac{r_B}{D_A/2}\right) \quad (1)$$

where $R_{sh}$ is the base sheet resistance, $r_B$ is the radius of the base contact. $R_{cir}$ will increase exponentially as the $D_A$ getting smaller due to smaller dimension/aperture design, resulting a higher RC time constant that will limit the device performance. The other issue for this layout is that the process will become very difficult once the device scales down to small diameter due to small via-hole and higher contact resistance, which causes the yield to be low. To avoid this problem, we have proposed a new layout designed to reduce resistance increase due to its lateral-feeding characteristics and geometry as shown in Fig. 2b. The resistance for this layout is then determined by the following equation:

$$R_{lat} = R_{sh} \times \frac{(d+t)}{L} \quad (2)$$

where $L$ is the emitter width, $d$ is the distance between base contact and emitter mesa, and $t$ is the intrinsic device width measured from the emitter mesa edge ($t < w$). From Eq.(2) we can design different geometry of $d$, $L$ and $w$ to maintain the lower resistance without sacrificing RC time constant, hence, the modulation speed, when we scale the devices.

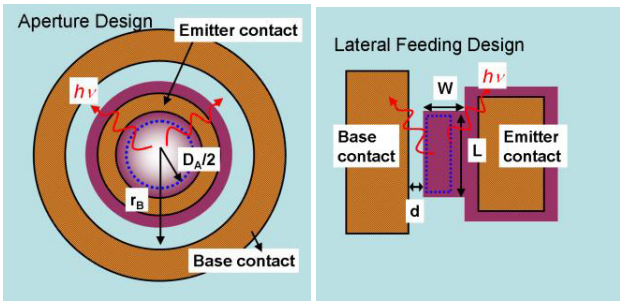


Fig.2 (a) aperture design (b) lateral feeding design

## LAYER STRUCTURE AND DEVICE FABRICATION

The epitaxial layers of the crystal used for the tilted-charge light emitting diode consist, upward from the substrate, a 3000 Å n-type doped GaAs buffer layer, a 500 Å graded $Al_{0.30}Ga_{0.70}As$ confining layer, a 213 Å graded $Al_{0.30}Ga_{0.70}As$ to $Al_{0.90}Ga_{0.10}As$ oxide buffer layer, a 595 Å n-type $Al_{0.98}Ga_{0.02}As$ oxidizable aperture layer and another 213 Å graded $Al_{0.90}Ga_{0.10}As$ to $Al_{0.30}Ga_{0.70}As$ oxide buffer layer. A 557 Å n-type GaAs contact layer, a 120 Å InGaP etch stop layer, and a 2871 Å undoped "drain" layer are grown on top. The "drain" layer is just beneath the 1358 Å base layer, which includes two undoped 112 Å InGaAs quantum wells and an $Al_{0.05}Ga_{0.95}As$ layer with average doping of $3x10^{19}$ $cm^{-3}$. The heterostructure emitter consists of a 511 Å n-type $In_{0.49}Ga_{0.51}P$ layer, a 213 Å graded $Al_{0.30}Ga_{0.70}As$ to $Al_{0.90}Ga_{0.10}As$ oxide buffer layer, a 595 Å n-type $Al_{0.98}Ga_{0.02}As$ oxidizable aperture layer, another 213 Å graded $Al_{0.90}Ga_{0.10}As$ to $Al_{0.30}Ga_{0.70}As$ oxide buffer layer, and a 500 Å graded $Al_{0.30}Ga_{0.70}As$ confining layer. The structure is completed with a 2000 Å GaAs top contact layer.

The tilted-charge LED is fabricated by first performing wet etching steps to form emitter and base-"drain" mesas, followed by an isolation etch from the sub-"drain" layer to the substrate. Metallization steps are then performed to provide the required electrical contacts. A diagram of the device in cross section is shown in Fig. 1. The completed LED has only two terminals: (a) a contact to the emitter layer, and (b) another across the base and "drain" layers. The base-"drain" forms a p-n junction with a reverse built-in field that is maintained by a common potential (zero potential difference) obtained via a common contact metallization extending to the base (Fig. 1). The zero base-"drain" potential difference ensures that there is no base

charge population density at the base-"drain" boundary, hence establishing a dynamic "tilted" emitter-to-"drain" population in the base. The "drain" layer performs therefore a role similar to the collector in a three-terminal HBLET. It allows excess minority carriers to be removed from the base ($I_D$), "swept" from base to "drain" by the built-in field at the base-"drain" p-n junction. Base carriers in transit from the emitter to the "drain" that do not recombine within the base transit time are removed "drained". This enables fast modulation of the tilted-charge LED by preventing the build-up of "slow" charge in the base. The tilted-charge LED possesses the high speed optical modulation characteristics of an HBLET.

## DEVICE CHARACTERISTICS AND RESULTS

Three different length of *L* (20, 10, and 5 μm) are fabricated and measured to investigate the parasitics in the proposed layout on the tilted-charge LED. The distance *d* between base/drain contact and emitter mesa is 1 μm while the emitter mesa width *w* is 5 μm for this study. From Eq.2 we expect to see lowest resistance for device dimension of 20x5 $\mu m^2$, but larger capacitance due to its largest emitter area. Figure 3 shows the L-I and I-V curve for these three devices, where the E20x5 $\mu m^2$ presents lowest resistance and highest optical output. The light output is measured using large area detector underneath the devices. The trun-on voltage of tilted-charge LED is determined by the emitter/base junction (forward bias) while the base/drain junction is slightly reversed due to its built-in voltage maintained by the common contact of base/drain. The light output is saturated due to higher current density and heat generation.

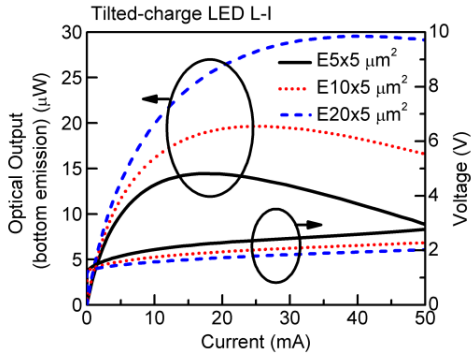


Fig. 3. Electrical and optical characteristics of different emitter mesa of tilted-charge LED.

The spontaneous optical modulation bandwidths for three different layouts under certain current density (20 $KA/cm^2$) are shown in Fig.4. The parasitics (R, C) can be simplified to only resistance effect because of biasing devices at same current density basically means the storage capacitance is similar for three devices; thus, the speed is limited by the resistance condition. The highest $f_{3dB}$ bandwidth of 3 GHz is observed for E20x5 $\mu m^2$ device at low current injection range (linear region of the L-I curve in Fig. 3).

Figure 5 shows the 3dB bandwidth at different current density for three devices. Although E20x5 $\mu m^2$ device possesses largest capacitance due to its larger active area, the smaller resistance seen at this layout help reduce the overall parasitics more, hence improve the high speed performance at lower current density. The 3dB bandwidth can be pushed higher if we operate it at higher current density level by saturating the QW and channeling (removing) the carriers faster.

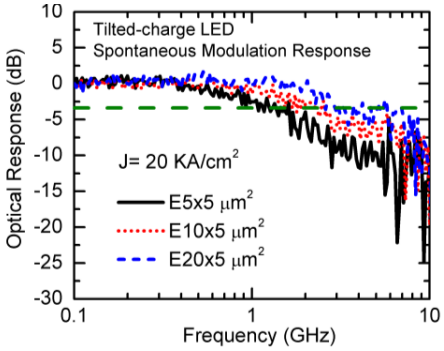


Fig. 4. Response of three different sizes of device under J=20 $KA/cm^2$ current density.

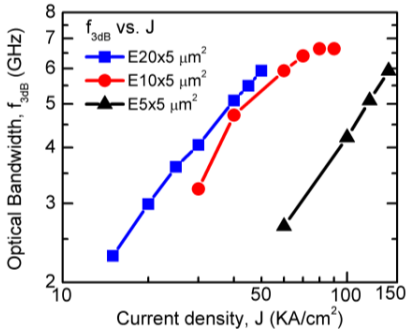


Fig. 5.Optical bandwidth vs. current density for three different devices.

## CONCLUSIONS

We have demonstrated a high-speed form of LED, tilted-charge LED, inheriting from the HBLET. The fast recombination process (sub-100 ps) is preserved in the LED form and can be modified and controlled by the layout design by improving (reducing) the intrinsic device characteristics (extrinsic parasitics, R and C). The proposed lateral-feeding layout can lead to multi-GHz operation with smaller resistance effect, and meanwhile provide simple (no oxidation process) and robust, high-yield process (larger area contact) compared to conventional aperture design layout.

ACKNOWLEDGEMENTS

M. Feng for the support of the Nick Holonyak, Jr. Chair of Electrical and Computer Engineering. G. Walter is grateful for the support of the Brain Gain Malaysia Diaspora (MOSTI) Program. The authors would like to thank Dr. Michael Gerhold (Army Research Office) and acknowledge the support by Army Research Office, Grant No. W911NF-08-1-0469.

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ACRONYMS

LET: Light-Emitting Transistor
LED: Light-Emitting Diode
HBLET: Heterojunction Bipolar Light-Emitting Transistor
VCSEL: Vertical-Cavity Surface-Emitting Laser