Backside Process Considerations for Fabricating Millimeter-Wave GaN HEMT MMICs

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Abstract

We describe a backside process for fabricating millimeter-wave GaN HEMT MMICs having a 0.1-μm length gate covered with a very thin SiN passivation layer, a thin epitaxial layer and airbridges. In particular, we discuss backside process issues regarding thin wafer support, SiC via-hole etching and wafer dicing. Finally, we demonstrate a W-band GaN low-noise amplifier with a record gain of 23 dB at 76.5 GHz and a noise figure of 3.8 dB at 80 GHz.

INTRODUCTION

The GaN HEMT, because of its excellent physical properties, is a high power device that shows great promise in a very wide range of applications, from power electronics to millimeter-wave communication [1]. In particular, various technologies are consolidated in millimeter-wave MMICs. We therefore optimized the epitaxial layer structure [2], front-side device process [3], backside via-hole process [4] and MMICs design [5] to produce millimeter-wave GaN HEMT MMICs. The via-hole is especially a key technology. However, if these technologies are not suitable, we will not be able to achieve the eventual manufacture of GaN HEMT MMICs.

In this paper, we describe backside process considerations for fabrication of millimeter-wave GaN HEMT MMICs.

OPTIMIZED EPITAXIAL LAYER AND FRONT-SIDE DEVICE

Figure 1 shows the schematic cross-sectional view of the millimeter-wave GaN HEMT. Fundamentally we used an n-GaN cap layer for the millimeter-wave GaN HEMT in order to suppress current collapse and to increase the Schottky barrier height [6]. We used a Y-shaped gate of length 0.1 μm for the millimeter-wave GaN HEMT [3]. This Y-shaped gate consists of a 0.1-μm fine gate and an over-gate, which is formed by electron beam lithography. Compared to the conventional T-shaped gate, the Y-shaped gate is well filled with the metal. The Y-shaped gate is therefore mechanically stronger and has a decreased gate resistance when compared to the conventional T-shaped gate. However, when a 0.1-μm gate was used, the conventional thick GaN buffer led to a short channel effect and large drain leakage current.

To optimize the epitaxial layer structure grown by metal-organic vapor phase epitaxy (MOVPE), we used a thin GaN channel and AlGaN buffer [2]. The thickness of the GaN channel was 250 nm and the proportion of Al in the AlGaN buffer was 5%. However, the reduction in the GaN channel thickness significantly degraded the crystal quality of the GaN HEMT epitaxial layer, resulting in an increase in current collapse. We therefore optimized the thickness of the AlGaN buffer by evaluating the yellow-luminescence (YL) and a root mean square surface roughness (RMS) using PL and AFM. Consequently, it was found that the YL intensity and RMS could be decreased by increasing the AlGaN buffer thickness up to 750 nm, and in this way the drain leakage current and current collapse of the millimeter-wave GaN HEMT were minimized.

In order to further improve the high frequency performance of the device, we used a very thin (50 nm-thick) SiN passivation layer to cover the gate [5]. As a result, the maximum stable gain (MSG)/maximum available gain (MAG) for 50 nm-thick SiN increased by 1-2 dB up to the W-band compared to 300 nm-thick SiN. This is because the parasitic gate-source capacitance (C_{gs}) and gate-drain capacitance (C_{gd}) were decreased by reducing the SiN thickness. In addition, the extrinsic current gain cutoff frequency (f_T) and maximum oscillation frequency (f_{max}) were 75 and 200 GHz for a device with a 50 nm-thick SiN passivation layer.

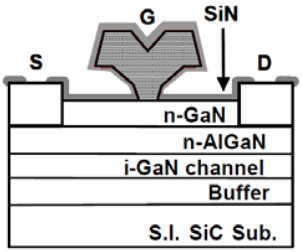

Fig. 1. Cross-sectional view of millimeter-wave GaN HEMT.

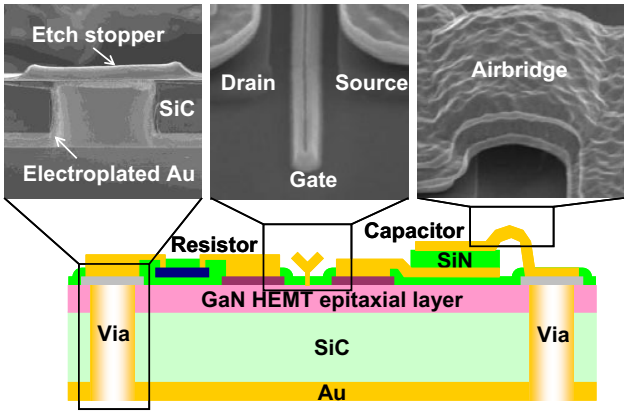

Fig. 2. Schematic millimeter-wave GaN HEMT MMICs.

As mentioned above, we optimized the epitaxial layer structure and front-side device. In addition, besides the transistors, millimeter-wave MMICs have passive components such as resistors, capacitors and interconnects including airbridges, as shown in Fig. 2. However, the manufacturing yield of GaN HEMT MMICs will decrease if these technologies are not suited to the backside process. In particular, the very fine Y-shaped gate electrodes covered with a very thin SiN passivation layer and the airbridges are mechanically very sensitive when the wafer is bonded to and debonded from the carrier. Furthermore, the undulating surface topology of the MMIC wafer is prone to generate the wafer microcracks during thinning. It is therefore necessary to deal very carefully with the backside process.

BACKSIDE PROCESS FOR MILLIMETER-WAVE MMIC

A. THIN WAFER SUPPORT

Figure 3 shows the flow chart for our GaN HEMT MMIC backside process. We have described the 3-inch SiC backside via-hole process elsewhere [4]. The SiC via-hole was fabricated from the backside of the wafer. Because a very thin (50-100 μm-thick), weak wafer is handled in the backside process, it is necessary to bond the front-side of the wafer to a transparent sapphire carrier plate with thermoplastic adhesive. Furthermore, for protection and planarization on the front-side surface, we used polymer that is resistant to high temperatures before the spin-coating of the adhesive. The protective polymer is indispensable for ensuring that scratches and microcracks are not generated when wafer thinning and debonding are carried out. However, it was found that this polymer affected the airbridges when it was being cured at a temperature of 300℃, which is considered to be higher than the wafer temperature during SiC high-rate etching. Table I shows the height of the airbridges measured with a confocal laser scanning microscope (CLSM). Consequently, the airbridges were crushed down by about 0.5 μm before and after bonding to the carrier, though short-circuiting of the interconnections was not seen. Although airbridges are found to be very effective for reducing parasitic capacitance and increasing breakdown voltage between the crossovers of the interconnects, they are not suited to the backside process.

B. SIC VIA-HOLE ETCHING

SiC via-holes are fabricated using inductively coupled plasma (ICP) etching. Details of the etching conditions are described elsewhere [4]. We reported several technical issues regarding SiC high-rate etching at 2 μm/min. First, we clarified the mechanism of pillar formation associated with micropipes and eliminated these pillars by reducing the operating pressure during etching [4, 7]. Furthermore, we found a large difference in the etching behavior between semi-insulating (S.I.) and n-doped SiC [8, 9], although the use of n-SiC, which is cheaper than S.I.-SiC, was preferable for optimizing the process conditions. As shown in Fig. 4, the etched bottom for S.I.-SiC was much rounder than for n-SiC. The height difference in S.I.-SiC between the center and edge of the via-hole bottom was approximately 10 μm. Therefore, when etching GaN HEMT/S.I.-SiC MMIC via-holes, the GaN surface appeared first at the center of the via-hole bottom, as shown in Fig. 5(a). As mentioned above, the optimized thickness of the GaN HEMT epitaxial layer for millimeter-wave applications was around 1 μm. Since the etch selectivity for GaN is 30 to 50, punch-through in the GaN HEMT layer was not observed until the SiC on the edge of via-hole bottom was completely etched, as shown in Fig.5(b). However, smaller GaN thicknesses may lead to punch-through in the center. Therefore, it is desirable that the via-hole bottom be flat.

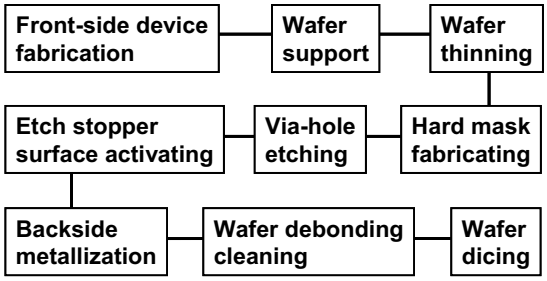

Fig. 3. Flow chart for GaN HEMT MMIC backside process.

Table I. Airbridge height measured by CLSM

Height / Airbridge	Initial(μm)	After process(μm)	Difference(μm)
No.1	2.70	2.07	0.63
No.2	2.27	1.84	0.43
No.3	2.36	1.77	0.59

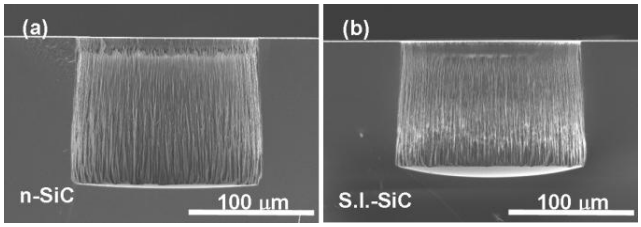

Fig. 4. Cross-sectional SEM images of 150 μm-diameter via-holes etched at the coil/platen powers of 2/0.3 kW: (a) n-SiC and (b) S.I.-SiC.

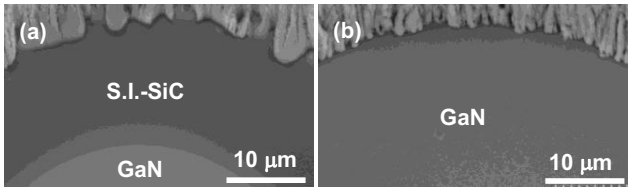

Fig. 5. SEM image of via-hole bottom for GaN HEMT/S.I.-SiC wafer.

Figure 6 shows the platen power dependence of the etch rate for both substrates at a coil power of 2 kW. The via-hole diameter was 150 μm. With both substrates, as the platen power increased, there was a corresponding increase in the etch rate. However, the etch rates for S.I.-SiC were clearly lower than those for n-SiC. Figure 7 shows the via-hole diameter dependence of the normalized etch depth in both substrates. The normalized etch depth is defined as the ratio of the etch depth to that of the 150-μm diameter hole. As a result, S.I.-SiC gave rise to a more significant RIE lag than n-SiC. According to our previous work [8, 9], this differential etching behavior can be attributed to the differences between the substrates in the wafer heating and negative charging of the sidewall during plasma etching. In n-SiC, the wafer temperature during etching became higher than in S.I.-SiC because of the higher free-carrier absorption coefficient. Therefore, the etch rate of the chemical reaction was enhanced in n-SiC. In addition, the negative charging in S.I.-SiC was larger than in n-SiC due to the low electrical conductivity. Therefore, in S.I.-SiC, a large number of positive ions are steered toward the sidewall, so that reducing the via-hole diameter decreases the number of vertically-incident ions more significantly resulting in a greater RIE lag than in n-SiC. Thus, the via-hole diameter must be unified in GaN HEMT MMIC wafers in order to obtain a high yield of via-hole fabrication.

We have described above several technical issues regarding SiC high rate etching. However, the point to which we paid most attention is whether the polymer and thermoplastic adhesive have sufficient tolerance to the wafer temperature, which rises during SiC high-rate etching. When the etch rate exceeds 2 μm/min, the thermoplastic adhesive becomes soft, causing the very thin (50-100 μm-thick) wafer to become wavy. Therefore, in our ICP system, the maximum SiC etch rate suitable for the MMIC process was 2 μm/min.

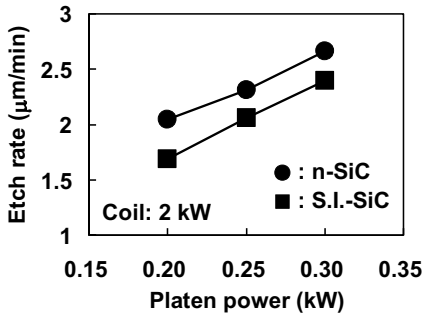

Fig. 6. Platen power dependence of etch rate for n-SiC and S.I.-SiC. The via-hole diameter is 150 μm.

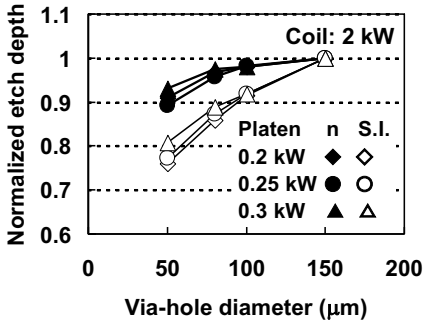

Fig. 7. Via-hole diameter dependence of normalized etch depth in both SiC substrates.

C. BACKSIDE PROCESS FOR DICING

Care must be taken with regard to dicing after the via-hole process. Figure 8 shows SEM images of a 0.1-μm gate length GaN HEMT with a 50 nm-thick SiN passivation layer after dicing. When dicing was performed without the polymer, a part of the 0.1 μm-length gate was lost, as shown in Fig. 8(a), as a result of the jet of water and high-pressure air used for removing particles, due to its mechanical weakness. However, when protected by the polymer, no loss of gate was observed, as shown in Fig. 8(b). As mentioned above, it is necessary to consider various points, regarding all aspects of the backside process, in order to manufacture millimeter-wave GaN HEMT MMICs.

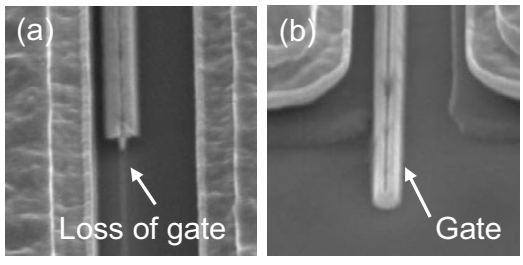

Fig.8. SEM images of 0.1-μm gate-length GaN HEMT with 50-nm-thick SiN passivation layer after dicing: (a) without polymer and (b) with polymer.

GaN HEMT MMIC PERFORMANCE

We fabricated W-band MMICs amplifiers using 0.12 µm-gate GaN HEMTs and grounded coplanar waveguides (GCPW) with via-holes [5]. Figure 9 shows a high-gain low-noise amplifier (LNA) that we fabricated. The size of the chip was 3.0 × 1.4 mm^2. The LNA had four stages with a 100-µm gate width GaN HEMT. When GCPW is used to design W-band MMICs, parasitic substrate modes, such as a parallel-plate (PPL) mode in the SiC substrate, greatly reduce the port isolation of the CPW MMIC and induce undesired feedback oscillation, especially for high-gain blocks. Therefore, we developed W-band MMIC amplifiers based on GCPW with via-holes. The array of via-holes within this chip was sufficient to reduce the excitation of the parasitic substrate mode up to the W-band.

Consequently, the fabricated LNA with via-holes achieved a record gain of 23.0 dB at 76.5 GHz, as shown in Fig.10. The source-drain voltage (V_{ds}) was 10 V. Moreover, the minimum noise figure (NF) of the LNA was measured to be 3.8 dB, with an associated gain of 20.4 dB at 80 GHz. We obtained an NF that is comparable to other GaAs- and InP-based devices having a gain of more than 15 dB in the W-band. This excellent result was achieved by integrating various technologies into GaN HEMT MMICs.

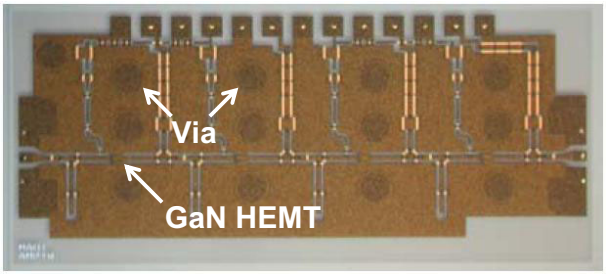

Fig.9. Photomicrograph of the fabricated MMIC LNA with GCPW. Its size is 3.0 × 1.4 mm^2.

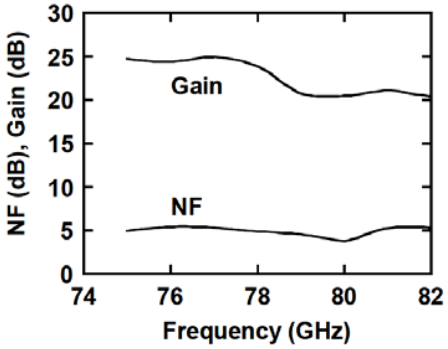

Fig. 10. Measured NF and gain of LNA (V_{ds}=10V)

CONCLUSIONS

We described a backside process for fabricating millimeter-wave GaN HEMT MMICs having a 0.1-µm length gate covered with a very thin SiN passivation layer, a thin epitaxial layer and airbridges. Backside process issues regarding thin wafer support, SiC via-hole etching and wafer dicing were discussed. Finally, we successfully demonstrated a W-band GaN LNA with a record gain of 23 dB at 76.5 GHz and a noise figure of 3.8 dB at 80 GHz.

ACKNOWLEDGEMENTS

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ACRONYMS

HEMT: High Electron Mobility Transistor
MMIC: Monolithic Millimeter-wave Integrated Circuit
PL: Photoluminescence
AFM: Atomic Force Microscope
SEM: Scanning Electron Microscope
RIE: Reactive Ion Etching