Evaluating pHEMT Process Improvements Using Wafer Level RF Tests

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Abstract

To increase production capacity, improve the performance of existing processes, and to introduce new, more advanced process technologies, processes must be evaluated using electrical tests. PCM's are used to evaluate the active transistor and passive device characteristics produced by the wafer process. DC testing of circuit designs is used to evaluate the success of the design, the success of the wafer processing, and the interaction of the design with the process. While good PCM and DC circuit test results are necessary, they are not sufficient to guarantee acceptable RF performance for products used in high performance RF applications such as cell phones. Consequently, RF testing is utilized to assure good RF performance. RF testing is performed at the package level. The time required to move product from wafer fab completion through package assembly delays feedback to the wafer fab process engineer. Adding wafer level RF tests provides quicker feedback and reduces the time required to complete a cycle of learning. This paper discusses the RF wafer probe tests used to evaluate the continuous improvements in Skyworks' pHEMT wafer process.

INTRODUCTION

Advanced cell phone architectures utilize high performance Front End Modules (FEMs) which integrate the HBT PA, multi-throw pHEMT RF switches, and passive filter components. The handset providers demand increasingly more difficult third harmonic and intermodulation distortion specifications with every new generation of product. The wafer fab processes must continuously improve to achieve high yield. Improvement requires change and changes must be rigorously evaluated. Electrical testing is used to determine if a process change is actually a performance improvement. Good wafer fab Process Control Monitor (PCM) and DC wafer probe tests are required. These measurements are relatively easy to make and are therefore quickly available to Process Engineering. However, wafer level DC tests do not necessarily guarantee acceptable RF module performance. The time required to move product from wafer fab completion through module assembly and test delays feedback to the wafer fab process engineer. Adding wafer level RF tests provides quick feedback and reduces the time required to complete a cycle of learning. Short cycles of learning are essential to problem solving and process development. In the experience of the authors, when it is difficult to obtain data, you get less of it. This paper discusses the various RF wafer test methods used to evaluate the continuous process improvements and capacity expansion in Skyworks' pHEMT wafer fab.

DISCUSSION

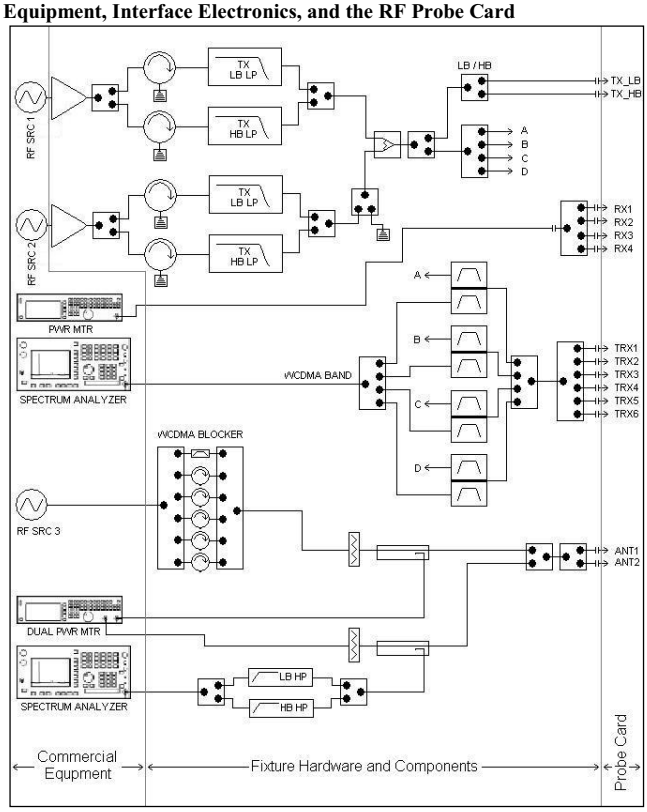
Wafer level tests employed by Skyworks include PCM and DC and RF wafer probe of the switch die. The PCM's are used to evaluate the active transistor and passive device characteristics produced by the wafer process. Both RF and DC PCM measurements are used to monitor the process. Further, the measurements enable RF device modeling parameters to be extracted for use by the circuit designers. DC testing of circuit designs is used to evaluate the success of the design, the success of the wafer processing, and the interaction of the design with the process. The circuit DC tests are Ion, Ioff, and Ileak of each arm of the switch. Ion and Ioff are the current of each of the switch arms when it is in the on and off conditions. Ileak is the gate leakage current of the switch arm when in the off condition. The wafer level RF circuit tests are insertion loss, second harmonics (2f0), third harmonics (3f0), leakage current, and intermodulation distortion (IMD). See reference [3] for a basic introduction to RF measurement terminology. The insertion loss is the amount of power in dB lost passing through the switch. Lower insertion loss translates into longer battery life by allowing the PA to provide less power into the switch to achieve the target power out of the switch. The isolation in dB between each arm of the switch is measured by applying power to one arm, and measuring the amount of power coming out of another switch arm that is biased to be off. The RF gate leakage current of a switch arm is measured by biasing the arm on, and measuring the amount of leakage current coming out of the gate of the switch arm under RF power conditions. Low gate leakage current over temperature is required to achieve good RF performance and long battery life. 2f0 and 3f0 are the unwanted second and third multiple of the fundamental (1f0) signal at the output of the switch. In cell phone applications, the output of the RF switch is typically directly connected to the antenna. Consequently, any harmonic signals at the output of the switch are transmitted. It is required that these spurious

signals be of a very low power so as not to interfere with communications. Generally, harmonic power must be less than -30 to -33 dBm (1 to .5 uW) power over worst case conditions of low battery voltage, high temperature, maximum transmit power, and an impedance mismatch at the output of the switch. Note: dBm is power relative to 1 mW. 0 dBm = 1 mW. IMD, measured in dBm, is the non-harmonic spurious signals added to the fundamental power signal. Like harmonics, lower IMD is better. IMD is measured by applying power to the input of the switch, while simultaneously applying power to the output at a different frequency. The power passed back through the input of the switch at the receiver frequency is measured. A real world case for IMD measurement is made by applying 1,950 MHz to the input of the switch, forcing 1,760 MHz into the output, and measuring the power at 2,140 MHz at the input of the switch. This is a good proxy for the full duplex transmit/receive WCDMA band I operation of the switch where the transmit frequency (TX) is 1,950 MHz and the receive frequency (RX) is 2,140 MHz. A spurious signal (blocker) of 1,760 MHz can be received on the antenna, passed to the RF switch, which can mix with the 2f0 of the transmit signal and generate a power signal at 2,140 MHz into the receiver and consequently interfere with the communication of information.

RX = 2TX – Blocker
RX = (2 * 1,950) – 1,760 = 2,140 MHz

A schematic of the RF test hardware is shown in Figure 1. On the left side of the schematic, a commercial ATE RF tester and/or commercially available bench instruments are utilized to source and measure the RF signals. On the right side of the schematic is the connection to the RF probe card. The probe card is designed to have 50 Ohm impedance, maximize the isolation between probe needles, and minimize the probe needles series inductance. The center section of the schematic is the custom designed and built interface hardware used to apply the desired RF power and frequency as well as select the desired frequency of the response. For cellular handset transmit switch applications, the RF signal source must cover a fundamental (1f0) frequency range of 824-1910 MHz and power levels up to +35 dBm (3.16 W). To accurately measure the device under test (DUT) harmonics, the RF signal from the power amplifier (PA) must be filtered of its harmonic contribution. On the measurement side, the high power 1f0 fundamental frequency needs to be filtered to get sufficient dynamic range to measure the DUT second and third harmonics (2f0 & 3f0). The schematic also includes hardware to measure the receiver (RX) out-of-band blocking performance of the DUT for full-duplex WCDMA signals. This IMD performance of the DUT requires measuring signals as low as -130 dBm (0.1 fW). Reference [4] is a gage study of the RF test hardware described above.

Figure 1 Schematic of RF Test Hardware Showing Commercial Test Equipment, Interface Electronics, and the RF Probe Card



RF wafer probe is performed on 100% of the RF switch die used in Skyworks FEMs. Insertion loss, isolation, leakage current, 2f0, 3f0, and IMD at the low band and high band fundamental frequencies used in cell phones in the range of 824 to 2,140 MHz are measured. The 2f0 and 3f0 measured are in the frequency range 1.648 to 5.73 GHz. An engineering RF probe test plan includes measurements over power, frequency, and control voltage. The engineering test plan can be run over temperature as well. Thus, probe test can provide a characterization of an RF switch in large quantities suitable for statistical analysis. Tens of thousands of switch die can be characterized. Wafer probe maps provide invaluable spatial information of RF performance across a wafer [1][2].

The DC and RF tests described above are utilized to evaluate process improvements and new equipment. With many cycles of learning, the process and epi conditions that produce superior RF performance can be identified [1]. Figure 2 shows data evaluating the effect of a change to the nitride process deposition conditions on third harmonics. The nitride conditions affect the density and lifetime of surface traps. Figure 3 shows data evaluating the effect of a change to the gate processing conditions on third harmonics. Figure 4 shows the effect of gate processing on switch arm leakage current. The gate process conditions influence the properties of the Schottky gate of the pHEMT as well as gate

leakage. Both have been found to influence the harmonic and IMD performance. Figure 5 shows the effect of Ohmic metal process conditions on the third harmonics [5]. The best process conditions for Ohmic metal, gate processing, and nitride deposition were combined and compared to the original process settings. The improved process (B) performed better at high power, low control voltage, room and 85C wafer probe test (Figure 6).

Figure 2 915 MHz Third Harmonic vs Nitride Deposition Conditions

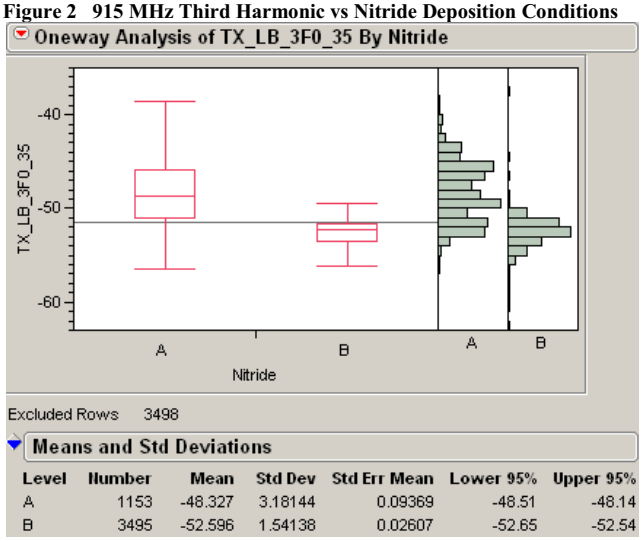


Figure 3 915 MHz Third Harmonic vs Gate Process Conditions

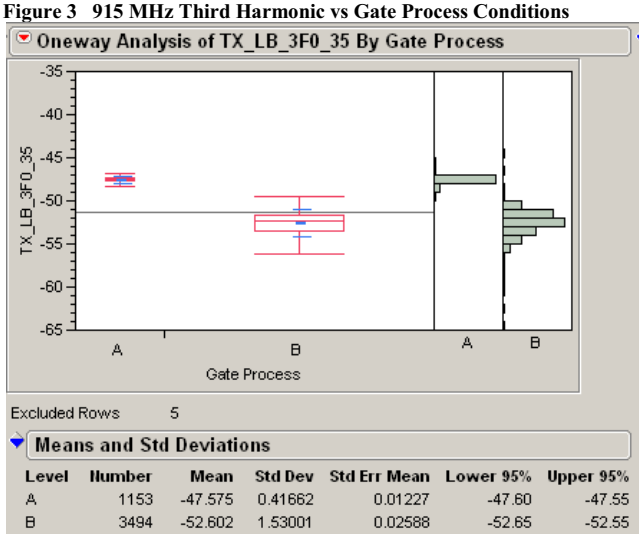


Figure 4 Switch Arm Leakage Current vs Gate Process Condition

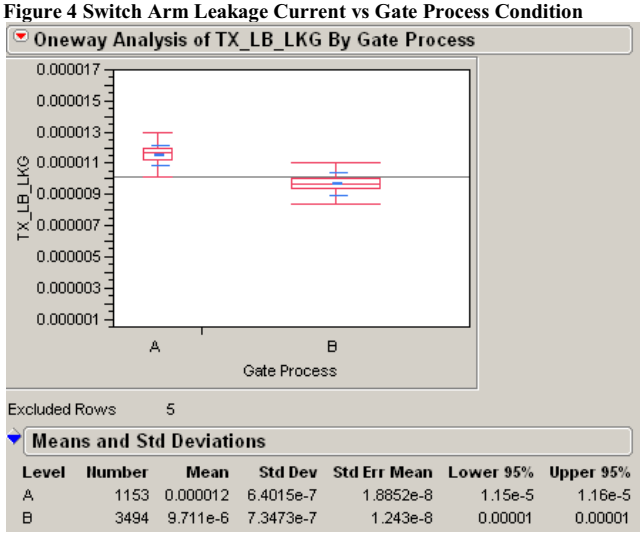


Figure 5 915 MHz Third Harmonic vs Ohmic Metal Process Conditions

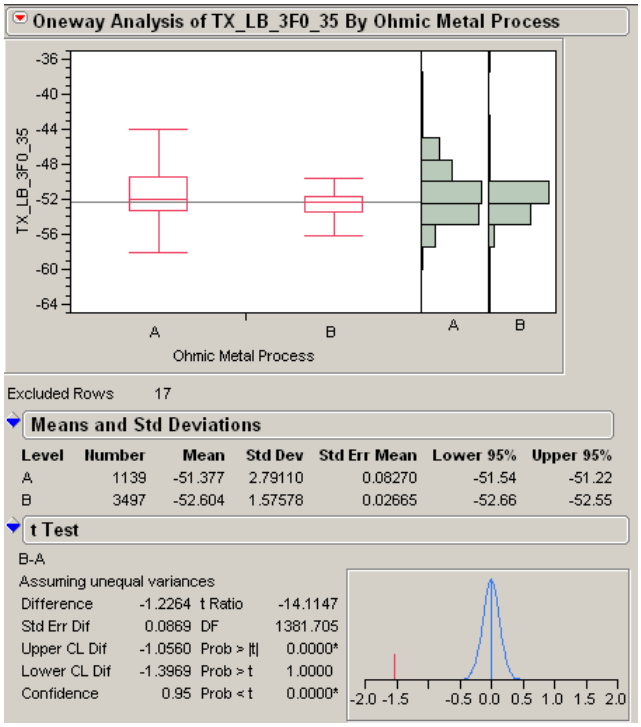
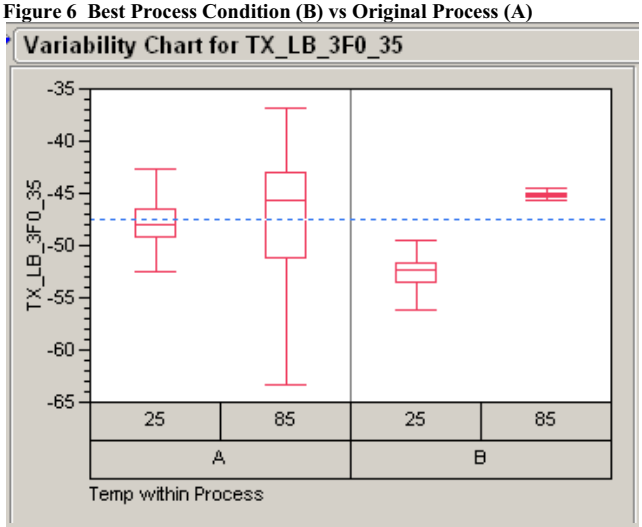


Figure 6 Best Process Condition (B) vs Original Process (A)



	Mean	Std Dev	Std Err Mean	Lower 95%	Upper 95%	Minimum	Maximum	Observations
TX_LB_3F0_35	-48.5478	4.349562	0.044997	-48.636	-48.4596	-76.8065	-19.5223	9344
Process[A]	-47.7715	5.160472	0.106634	-47.9806	-47.5624	-76.8065	-19.5223	2342
Process[B]	-48.8075	4.009195	0.047912	-48.9014	-48.7136	-67.7661	-22.9068	7002
Process[A] Temp[25]	-47.6615	2.480942	0.0725	-47.8038	-47.5193	-53.556	-20.4667	1171
Process[A] Temp[85]	-47.8815	6.863267	0.200564	-48.275	-47.488	-76.8065	-19.5223	1171
Process[B] Temp[25]	-52.5762	1.777152	0.030035	-52.6351	-52.5173	-67.7661	-23.9377	3501
Process[B] Temp[85]	-45.0388	0.761247	0.012866	-45.0641	-45.0136	-52.6288	-22.9068	3501

CONCLUSIONS

Wafer level RF testing provides process engineers with critically needed test results much faster and more frequently than can be obtained from packaged parts. The increased availability of this information facilitates an increase in the number of wafer fab experiments that can be evaluated. Consequently, continuous improvement can occur at a faster rate.

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ACRONYMS

pHEMT: Pseudomorphic High Electron Mobility Transistor
PCM: Process Control Monitor
PA: Power Amplifier
FEM: Front End Module
1f0: Fundamental frequency
2f0: Second harmonic
3f0: Third harmonic
IMD: Intermodulation Distortion
TX: Transmit
RX: Receive
DUT: Device Under Test