Quilt Packaging: A robust coplanar chip-to-chip interconnect offering very high bandwidth

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Abstract

A novel coplanar waveguide-based chip-to-chip interconnect scheme called Quilt Packaging (QP) has been developed. This technology enables extremely high speed integration of multiple chips on Si substrates. The demonstration of this technology in GaAs and InP is ongoing. With this technology, wiring delays associated with signal transmission from chip to chip are greatly reduced. The mechanical properties of QP at elevated temperatures are under study to improve reliability.

INTRODUCTION

Quilt packaging (QP) [1-6] is a novel interconnect technology that offers very high throughput coupled with short wire delays, compared with wire and bump bonding and package interconnects whose inductance and capacitance can cause signal distortion and unwanted resonances.

Quilt packaging makes use of coplanar waveguide (CPW) structures along the edge of each chip that are extended a short distance off the edge of the chips and joined by solder. These coplanar waveguide extensions, or "nodules," are reinforced for ruggedness by etching and anchoring into the substrate. The coplanar waveguide interconnects may be arbitrarily shaped by photolithography to improve broadband signal integrity. This lithographic control allows nodules to be packed as densely as mechanical strength and electrical coupling considerations allow.

Previous papers have discussed microwave measurements on joined silicon chips. This article discusses QP integration, interconnecting chips on GaAs substrates with those on other III-V substrates or with Si.

The technology is illustrated in Figs. 1-3. Figure 1 shows a concept for a QP system, illustrating a system that makes use of the best properties of circuits fabricated in several different material systems. Figure 2 is a rendering of a quilted system comprising three smaller chips, and Fig. 3 shows its realization for a coplanar through-line on two abutting chips.

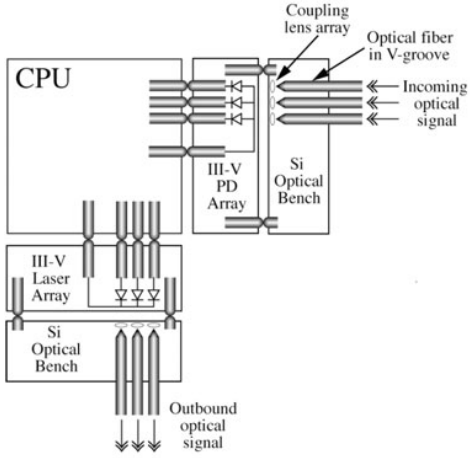


Figure 1: Concept of several technologies interfaced by QP to use the best qualities of each, optimizing performance of the overall system.

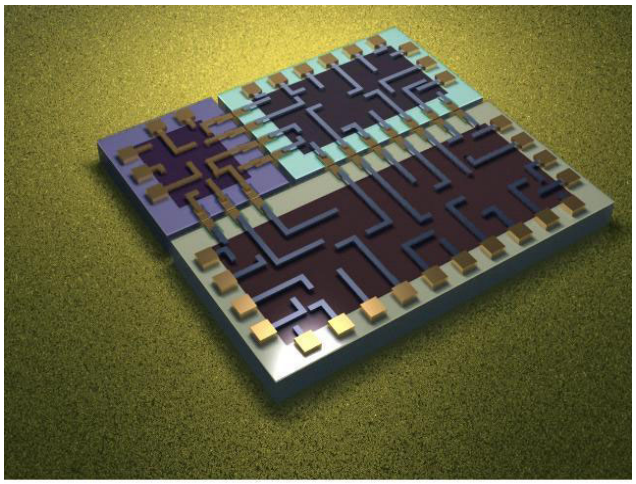


Figure 2: Rendering of a "metachip" –three chips interfaced by high speed QP interconnects.

PROCESS TECHNOLOGY

Chip-to-chip interconnects were built on silicon to verify device performance. A micrograph of a finished interconnect between Si chips is shown in Fig. 3. Figure 4 shows a detail of the mating face of a single chip, with ground lines surrounding a 10 µm wide, 20 µm deep signal line.

A similar structure is proposed for manufacture on semi-insulating GaAs. The method currently under development is as follows. A one-micron thick layer of PECVD silicon dioxide is deposited, windows are opened using photoresist and buffered HF, and the substrate is etched in an inductively coupled Cl_2/Ar plasma (Oerlikon ICP790) to cut nodule-shaped trenches in the substrate. The substrate is conformally coated with an adhesion layer of Ti and a thin seed of Cu to permit electroplating. The trenches are filled with copper (Intervia Cu, Transene), and this copper is polished flush by lapping using lapping papers of increasing fineness. (Work currently is done on small pieces, but on full wafers, chemical mechanical polishing of the substrates is more ideal and is under development). Interconnects are deposited by evaporating one micron of copper (Temescal FC-1800 evaporator) and liftoff using image-reversing AZ5214 photoresist. A PECVD oxide hard mask is applied onto the wafer, and the wafers are reinserted into the inductively coupled plasma to dice into chips and undercut nodules. A photoresist layer is applied to protect the chip surface while exposing the ends of the nodules. The nodule edges are then coated with immersion tin (using Technic, Inc.'s LEVELTECH process). The chips are aligned with applied pressure, and the tin is reflowed to solder together.

The fabrication on GaAs is has to date been completed up to the on-chip metallization step, but the dicing etch has not been perfected to yield the desired degree of nodule undercut. Copper nodules inlaid 15 µm deep into GaAs and InP by electroplating and polishing are shown in Fig. 5.

SIGNAL TRANSMISSION

The accurate lithographic definition of the interconnect geometry allows excellent control over the electrical performance of QP nodules. The shape of the nodules can be easily optimized to improve signal integrity. Test transmission lines were first measured on silicon. Figures 6-7 illustrate the electrical performance. The interconnection between one chip to the next (labeled "Nodules" in Fig. 6) adds a delay time of no more than 2.7 picoseconds relative to a through line standard on the same wafer (labeled "Through" in Fig. 6). Fig. 7 illustrates that the chip-to-chip QP interconnect adds very little insertion loss over the entire range of 50 MHz to 110 GHz, relative to an on-chip through line.

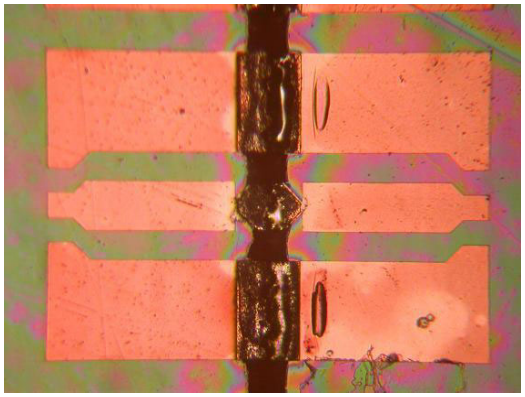


Figure 3: Realization of CPW connection between silicon chips, showing a detail of a coplanar waveguide extending from one chip on the left to a second on the right.

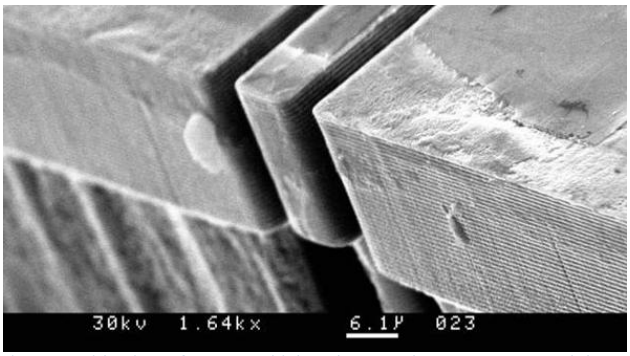
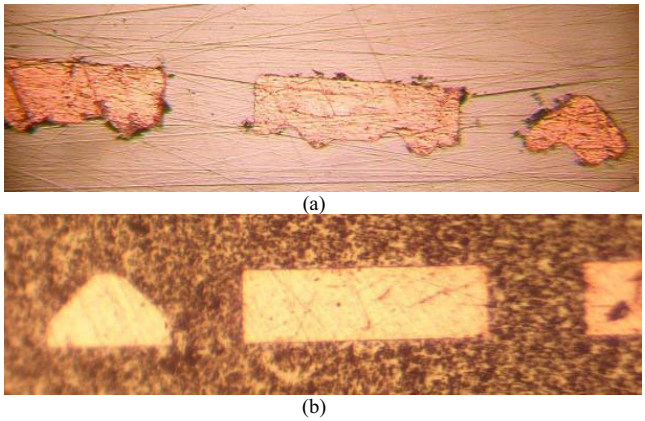


Figure 4: Side view of a 10 µm thick and 20 µm deep copper QP nodule on silicon substrate.



(a)

(b)

Figure 5: Copper inlaid and planarized by lapping for QP test structures on (a) InP and (b) GaAs. These inlaid structures will form nodules like those in Fig. 3.

Simulation was performed on GaAs to estimate the expected electrical performance. Figure 8 shows the predicted insertion loss for a QP connection between two GaAs chips, using Ansoft HFSS for simulation. Simulation

predicts an insertion loss of less than 0.5 dB to 110 GHz can be expected.

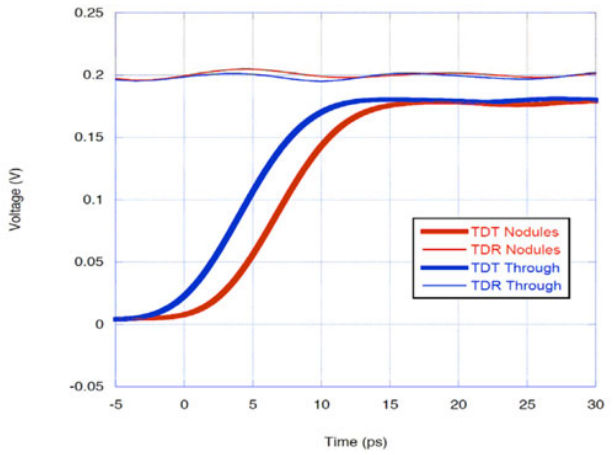


Figure 6: Measured time-domain reflection and transmission data, showing that the reflection is small, and that the delay due to the chip-to-chip transmission adds 2.7 ps to the through measurement.

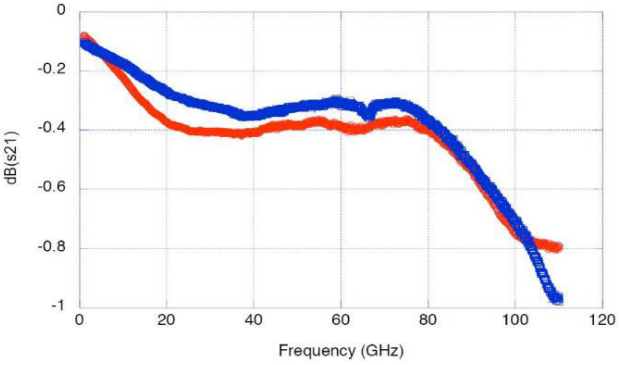


Figure 7: The transition from chip to chip (red curve) adds very little insertion loss to the through measurement (blue curve) between 50 MHz and 110 GHz.

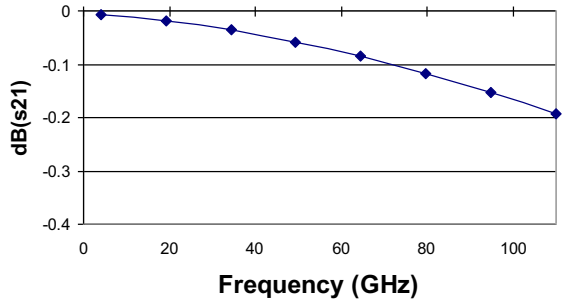


Figure 8: Predicted insertion loss (using Ansoft HFSS) for an optimized nodule line on GaAs, as a function of frequency.

THERMAL PERFORMANCE

Thermal simulations were performed to study mechanical reliability at elevated temperature. COMSOL Multiphysics simulations were performed of two chips attached with epoxy to a carrier wafer made of bismaleimide triazine, which features low dielectric constant and high glass transition temperature. The chips have copper encased in oxide insulation. The resulting von Mises stress in the oxide and copper lines are normalized to the ultimate stresses (220 MPa for copper and 50 GPa for silicon dioxide); a normalized von Mises stress of unity indicates failure.

Representative results are shown in Fig. 9. GaAs and Si have significantly different thermal expansion coefficients (6.9 and 2.6, respectively), so if nodules bridge the gap between dissimilar chips (GaAs-Si), the stress in the oxide is considerably higher than if each chip is of the same type (GaAs-GaAs) or (Si-Si).

COMSOL simulations indicate that the first point of failure is always at a sharp corner of the copper-oxide interface. Further simulations show that geometrically softening these corners significantly reduces the stress. Small modifications to the fabrication process can be introduced to produce such rounding, but SEM imaging shows that a small amount of unplanned edge rounding already occurs automatically. This rounding is believed to be caused by sidewall-induced ion shielding during the inductively coupled plasma etch.

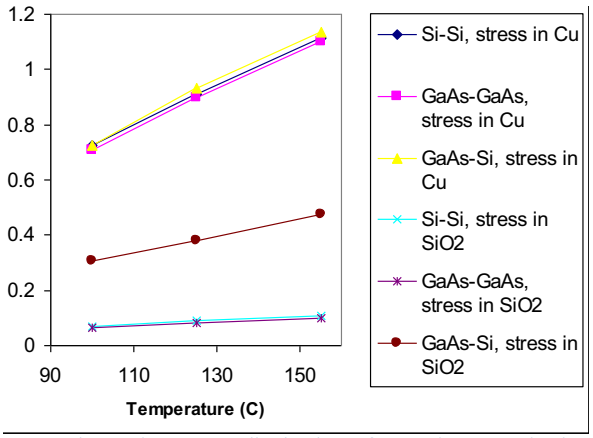


Figure 9: The maximum normalized values of von Mises stress is plotted for each combination of chip connections. The von Mises stress in the copper is normalized to 220 MPa, while the stress in the oxide is normalized to 50 GPa.

CONCLUSIONS

Quilt packaging is an enabling technology that provides robust, high speed chip-to-chip connections on Si and promises to do the same on GaAs and other III-Vs. Process development for heterogeneous integration of Si and III-V substrates is underway, and the thermal properties of such heterogeneous systems are under investigation.

ACKNOWLEDGEMENTS

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ACRONYMS

CPW: Co-planar Waveguide
QP: Quilt Packaging
PECVD: Plasma-Enhanced Chemical Vapor Deposition
ICP: Inductively-Coupled Plasma