SESSION 10: PROCESS ETCH

Chairs: Russ Westerman, *Plasma-Therm LLC,* and Chris Yousey, *Microlink Devices*

Papers in this section focus on practical problems that arise during wet and dry etching of compound semiconductors and the solutions used to overcome them. The first paper of the session by Skyworks Solutions discusses a yield loss problem related to a dry etch process for polyimide vias. The cause of the yield loss was found to be a reduction in process margin due to an interaction between a resist material change in conjunction with substrate heating during a dry etch process. The second paper in the session by the U.S Army Night Vision & Electronic Sensors Directorate investigates the use of optical emission spectroscopy (OES) during the dry etch of HgCdTe devices. Relative emission intensities for various reactants and etch products are correlated to etch performance in an effort to understand the interaction of resist profiles, materials and plasma parameters during HgCdTe device processing. The next paper by Plasma-Therm also looks at using plasma emission to control compound semiconductor dry etch processes. The theory, application, and limitations of optical emission interferometry (OEI) are described along with data demonstrating the capability of OEI to endpoint etch processes at specific material interfaces after a given etch depth into a material has been achieved. The final two papers of the session focus on wet etch processes. Cobham looks at yield losses during microwave FET processing due to electrochemical etching near the transistor gate. Information related to the process sequence as well as the corrective actions to the process are disclosed. In the final presentation, a team from Sandia National Labs looks at surface treatments to improve wet etch performance during base-collector formation for HBT fabrication. A NH_4OH based pretreatment to remove native oxides prior to lithography was found to improve resist adhesion, sidewall profile, and ultimately the step coverage of subsequent interconnect metallization.