SESSION 4: DEVICE TECHNOLOGY

Chairs: Kamal Alavi, *Raytheon Corp.*

The Device Technology session has four regular papers and one interactive one, all having practical and relevant information for III-V device engineers. The first paper, from WIN, addresses the fabrication of high-yield 0.25um optical gate power pHEMTs at 8V drain bias, where low output power drift is achieved through epitaxial layer design optimization. The second paper, from IIT, India, and National Chiao Tung University, Taiwan, discusses a composite channel mHEMT with 78% Indium mole fraction for W band applications. The third paper, from GCS, details the performance status, and capabilities of double heterojunction InP/InGaAs foundry processing with fT and fmax higher than 250 GHz. The last paper, also from WIN, discusses the epitaxial design and device geometry for fabrication highly linear and thermally stable 0.5um optical gate FETs for wireless infrastructure applications. An additional paper on Device Technology is included in Thursday's poster session. The poster from Ulm University, in Germany, details the important topic of photoresist profile control for sub-0.5um T-gate formation using conventional i-line lithography tools.