SESSION 8: PROCESS METAL

Chair: Paul Werbaneth, *Tegal Corp.*

CS MANTECH, as a conference, is all about compound semiconductor *manufacturing* technology, and, in this year's metallization session, the emphasis is squarely on papers and topics from some of the world's powerhouse fabs reporting on the robust, cost-effective, solutions these fabs and engineers have developed to increase the productivity and yields of the metal processing steps employed in High Volume Manufacturing of III-V devices today. In the metallization session's first paper, Northrop Grumman Space Technology describe how wafer level bump technology developed on the silicon-side of the world can be successfully ported over into a III-V MIMIC backside metallization process. The benefits of wafer bumping include enabling both chip-level and wafer-level assembly of the MMIC devices, which reduces the overall assembly cost and enhances the RF performance of the "bumped" devices. In the second paper of this session, TriQuint Semiconductor report on their successful efforts to develop I-line negative photoresist lift-off processes for producing the very fine interdigital transducer metal structures that are the defining features of Surface Acoustic Wave devices. TriQuint's target: clean, wing-free liftoffs. Their results: SAW filter duty factors within 2% of target, and excellent liftoff process capabilities across a range of feature sizes. Converting TaN reactive sputter deposition processes from a batch tool to a single wafer tool is a project in itself. Converting TaN reactive sputter deposition processes from 4" wafers to 6" wafers? Another significant project. Doing both at the same time in a production environment? That's one for the professionals, and the subject of the third paper in this metallization session, presented by Skyworks Solutions (West Coast). The fourth paper in this session, from (East Coast) Skyworks Solutions, tells how Skyworks developed novel measures to prevent excessive cross-linking in lift-off photoresists as a result of secondary electron emission during lift-off metallization. The excessively cross-linked photoresist doesn't strip well, so residues seen post-strip can be directly correlated to the amount of secondary electron generation during E-beam metal evaporation – a valuable observation, and one necessary for reducing the amount of said post-strip residues, thereby increasing device yields and reducing fab cycle times. The Metallization Session finishes with a talk from Avago Technologies and WIN Semiconductor on improved emitter resistance achieved through using barrier metals in an InGaP HBT process. Using STEM and flyback measurement techniques, Avago and Win show how sputtered barrier layers of either TiW or W affect the stability of InGaAs – barrier metal – Ti interfaces, and how the barrier layers reduce mean flyback resistance, and also greatly improve the overall distribution of the flyback resistance results.