Balancing Electrical and Thermal Device Characteristics – Thru Wafer Vias vs. Backside Thermal Vias

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Abstract

Device design and process strategies improving the circuit thermal stability by lowering the device junction temperature, while minimizing the device thermal resistance, are examined. We investigate adding thick (up to 4 µm) metal layers on top of the HBT device, moving TWVs closer to the device, and using thermal vias. The results show that most of the thermal resistance improvements are obtained if thick metal is used on top of the device, while the TWV plays a less important role. In addition, this work shows that thermal vias have limited use since they degrade the device RF performance.

INTRODUCTION

InGaP/GaAs and SiGe heterojunction bipolar transistors (HBT) are widely used for wireless applications since they have excellent features such as high power density and high efficiency. The high power dissipation per unit area requires careful thermal management. There are both circuit design strategies and manufacturing/process approaches to improve the circuit thermal stability by lowering the device junction temperature or minimize the device thermal resistance.

The device design/process strategies include “flip-chip” bonding, using metal heat shunts[1], thru-wafer via (TWV) holes connected to the device through large metal plates[2], collector-up HBTs with emitter connected directly to a heat-sink through a thru-wafer via[3], or use of partial vias[4,5].

Metal heat shunts [1] can reduce the device thermal resistance by more than half without degrading the RF characteristics, but this method is mostly applicable to high power GaAs FET devices where the device extents in excess of 500 µm due to the dimension of the multiple TWVs. The size of our HBT devices makes this strategy difficult to implement. Adding multiple TWVs around the device and connecting those to the HBT’s emitter proves to lower the thermal resistance but it requires considerable real estate[2]. The use of partial thru-wafer vias (backside thermal via, BTV) [4,5] was also proven to lower the device thermal resistance. However, previous studies did not discuss the impact of the additional capacitance, created by the proximity of the BTV, on the RF performance

In this work we investigate both the use of front–side metal as heat dissipation paths to adjacent TWV and the use of BTVs. Figure 1 displays the two approaches graphically. In the first case, we investigate the use of either Au or Cu as the TWV metal, with various top metal (Au) thicknesses while varying the distance between the TWV and the device.

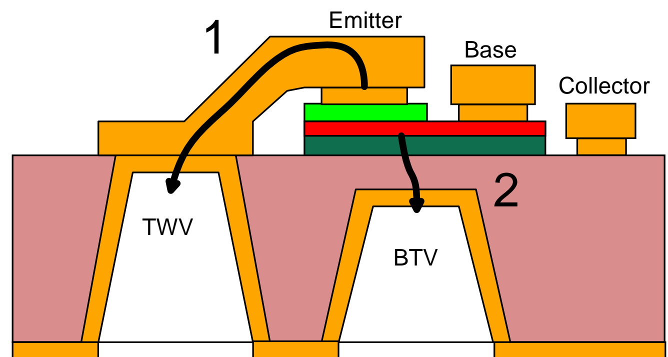


Figure 1. Two approaches to heat sinking.

The second approach (backside thermal via, BTV) involves partially etching vias through most of the GaAs substrate (2) and covering the sidewalls with Au in a typical thru-wafer via process.

TWV STRUCTURES

The devices fabricated for this study consist of InGaP HBTs with an emitter area of 120 µm^2, built in RF probeable test patterns on wafers processed in Skyworks Solutions Newbury Park GaAs Fab. The device emitters are connected to the backside ground metal (approx. 5 µm thick) through a top metal plate and through TWVs (approximately 40 µm in diameter) placed at various distances away from the device (Figure 2). The samples were laser-scribed and bonded with epoxy (Au backside samples) or soldered (Cu backside samples) to a heat sink. Variables in this experiment were the thickness of the top metal plate, the distance between the TWV and the device (between 15 µm and 70 µm), the choice of backside metallization (either Au or Cu), and the die attach - solder in the case of Cu samples or epoxy. The thickness of the top metal plate was varied by

using either M2 (second level metal interconnect) of about 2 µm, or M2+M3 (both second and third level metal interconnect) for a total of approximately 4 µm of Au.

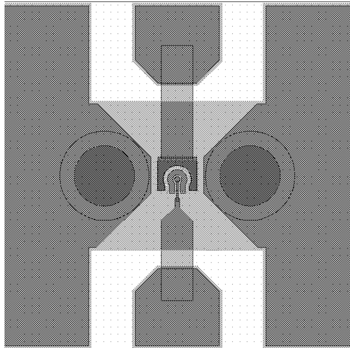


Figure 2. Sample layout of TWV devices. Two TWVs are placed at various distances from the device).

Five samples of each variant were tested. Electrical tests include DC, RF up to 6 GHz and thermal resistance. Figure 3 shows the average thermal resistance of each variant. The TWV proximity to the device has little impact. Similarly, the choice of either Au or Cu backside metal or the use of solder instead of epoxy results in very little change in thermal resistance. However, the use of thicker metal plates on top of the device shows a 17.3% drop in R_{th} overall. The lower R_{th} samples do not show a significant improvement in RF characteristics (Figure 4), mainly because these standard RF test conditions do not use high enough current density for the effect to show up. However, the lower R_{th} samples did display an increased current density by 20% at the maximum DC gain (Beta) point (Figure 5). This allows the device f_T and RF gain to peak at higher current density as well, which should improve the device's linearity and power added efficiency. This should also yield much more thermally stable device characteristics.

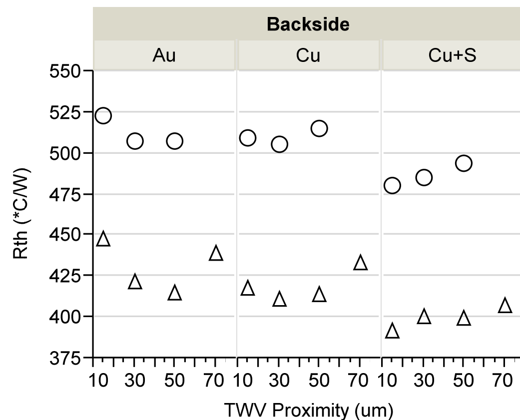


Figure 3. Thermal improvements are best with thicker metal; very little dependence of the TWV proximity is observed (Δ - M2+M3 plate, O – M2 only).

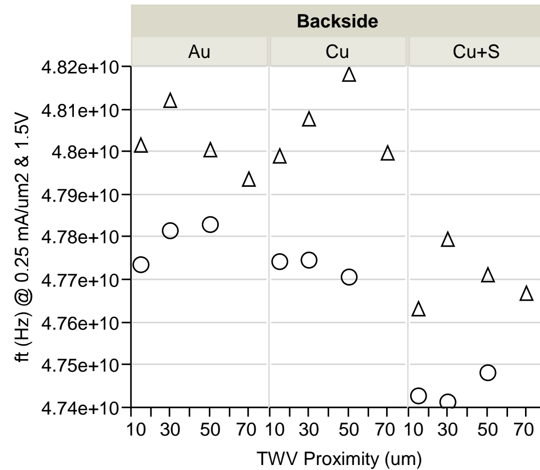


Figure 4. Devices with thicker top metal show higher Ft at high current densities (Δ - M2+M3 metal plate, O – M2 only).

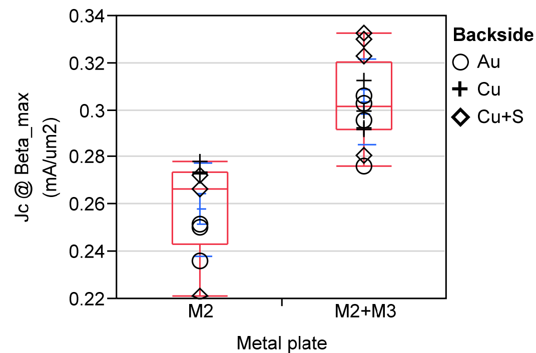


Figure 5. Collector current density at maximum Beta increases by 20% with the addition of M3 layer.

BTV STRUCTURES

For the evaluation of backside thermal vias, the devices did not use top metal plates as in the previous design, to increase the importance of the thermal resistance through the substrate. In addition, TWVs were partially etched. Previous studies used an etch-stop layer to stop the via etching at a specific distance to the active device layers[4,5]. In our work, we intentionally varied the distance between the top of the via and the device. To accomplish this, a multiple etch-stop layer is not feasible nor was running multiple wafers. However, we modified our standard wafer and TWV etch process combined with structures designed with various via diameters and this resulted in partial TWVs which stopped farther from the device if smaller layout diameters were used. The standard TWV process shows the TWV with a drawn diameter of 28 µm fully etched. Since the TWV is placed directly underneath the device, these devices were

completely shorted electrically (because the TWV extended to the collector layer of the device). Figure 6 displays an example of a backside thermal via underneath the device.

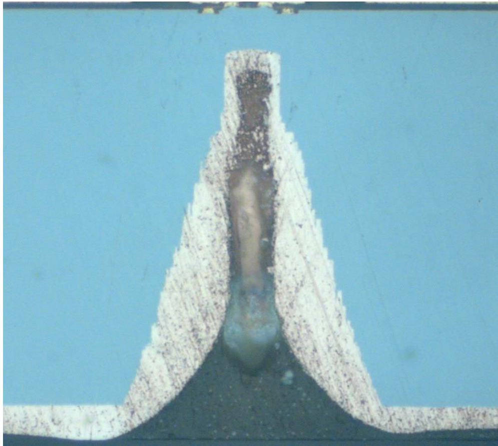


Figure 6. Partially etched TWV (backside thermal via).

Figure 7 shows thermal resistance results of five samples each from devices with drawn TWV diameters between 26 µm down to 18 µm. The results show modest improvements in device thermal resistance for samples up to 24 µm in diameter, with significantly lower values and higher variation only for the 26 µm devices. This data shows that meaningful thermal improvements can be achieved only with aggressive BTVs, with very little material left between the top of the via and the device.

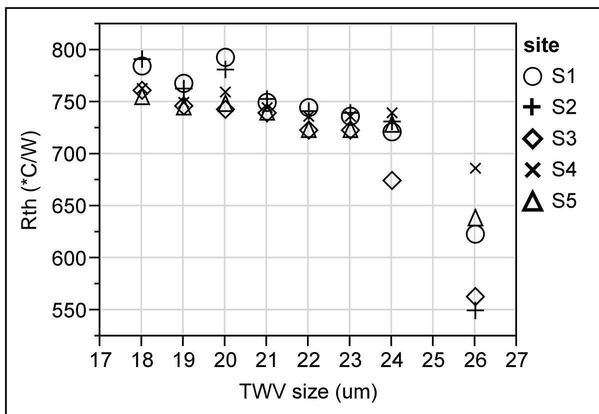
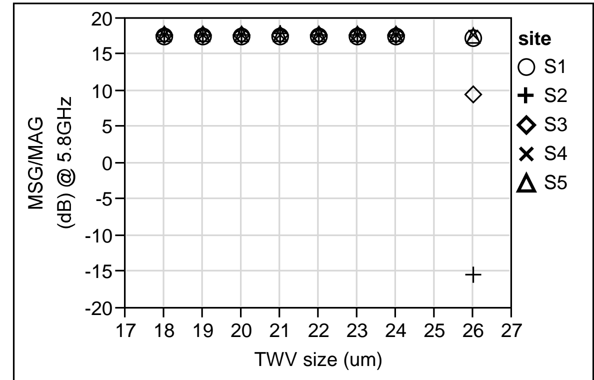


Figure 7. Modest improvements in device thermal resistance are achieved except for vias very close to the device.

The proximity of the top of the BTV to the device raises concerns regarding the parasitic capacitance since the BTV is lined with either Au or Cu, especially since the devices are normally used in common-emitter configurations. Figure 8 shows no statistically significant different RF small signal gain for the devices except if the BTV is very close to the device, in which case the gain degrades.



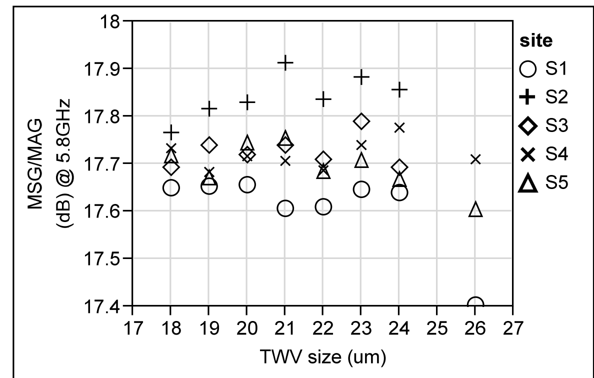


Figure 8. Gain collapse of structures with BTV very close to device. Second plot represents a rescale of the first plot excluding the gain-collapsed devices.

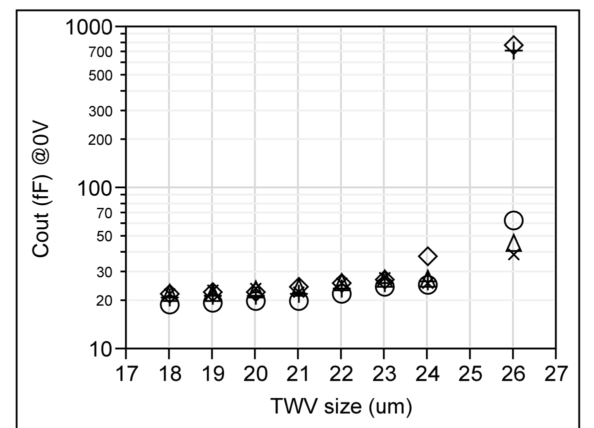


Figure 9. Device parasitic capacitance increases with BTV-to-device proximity.

A closer look at the measured output capacitance Cout (collector-emitter capacitance) at device cold condition (0 V) shows the parasitic capacitance of the degraded gain devices to be significantly higher than normal (Figure 9), by almost

two decades to 800 fF from 20 fF. A quick calculation of the parasitic capacitance between the device and the BTV based on the area of the BTV top metal plate and the GaAs permittivity shows that the 26 µm BTV has to be below 5 µm away from the device to achieve this output capacitance. Sample cross-sections of the 26 µm and 24 µm devices show a 2.5 µm and 8.5 µm distance between the top of the via and the device, respectively. The capacitance is further increased by the roughness of the top via surface. These results show that such distances away from the device are hard to achieve with this TWV process, while using an etch stop layer adds process and epitaxial growth complexity. More importantly, they show that meaningful thermal improvements are not achievable without the degradation of the device RF performance for common emitter topologies.

COMPARISON OF THE TWO METHODS

The results provided by this work show that significant thermal resistance improvement is obtained if thick metal is deposited on top of the device and connected to the device's emitter. The thermal via approach provides only as much as a 4% improvement in R_{th} without degradation of the device's RF performance. In absolute value, the devices with thermal vias have a 70% larger thermal resistance than devices with thick top metal plates. The backside thermal via approach, at least for our current process and device design, as opposed to large power FET devices[1], does not provide much benefit

In the case of devices with top metal plates, we showed that the addition of a TWV in close proximity to the device and electrically connected to the shunt plate does not improve the thermal resistance. Instead, the addition of the thick metal shunt is the significant factor. This is a surprising result given the literature[2]. However, previous studies failed to split the influence of the metal plate and the TWV separately. In addition, they use TWVs with much larger features compared to those of this work.

The use of thicker top metal heat shunts proves significant not only in lowering the individual device thermal resistance, but also in building a more uniform temperature profile across an array of devices with a common emitter.

A uniform thermal distribution across the array minimizes the probability of thermal collapse due to current crowding on the hotter devices.

CONCLUSIONS

This work shows that most of the thermal resistance improvements for our production HBT process are obtained if thick metal is used on top of the device up to less than 4 µm as a heat spreading shunt, while very little improvement is seen if TWVs are connected to the shunt and the wafer backside metal as a heat dissipation path, even if in close proximity to the device. Moreover, this work shows the limitations of the backside thermal via approach to improve the device thermal properties without degradation of its RF characteristics due to parasitic capacitive effects.

ACKNOWLEDGEMENTS

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ACRONYMS

HBT: Heterojunction Bipolar Transistor
TWV: Through-Wafer Via
BTV: Backside Thermal Via
R_{th}: Thermal Resistance

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