

The Study of Heterojunction Bipolar Transistors for High Ruggedness Performance

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Abstract

InGaP/GaAs HBT has been widely used in power amplifier (PA) design for wireless communications due to its high linearity and high efficiency. For in the application of GSM power amplifier, it is at risk of being damaged due to high voltage standing wave ratio (VSWR) mismatch. To increase the capability of the device ruggedness, varieties of collector designs with proprietary collector doping profiles have been developed. In this paper, we will present the study for evaluating the device ruggedness performance through experimental verification.

INTRODUCTION

For the using of an HBT as GSM power amplifier, it is essential that a power amplifier does not fail at high load VSWR conditions due to the unpredictable antenna load. To satisfy this requirement, sufficiently high collector-emitter breakdown voltage is needed. One of the approaches is to increase in a collector thickness more than 2 μm empirically, which could lead to a higher breakdown voltage (off-state breakdown voltage) [1]. However, thicker collector degrades the device performance such as resulting in high collector resistance and also raising the process difficulty owing to high collector topology. On the other hand, the studies announced that the on-state breakdown of devices can be improved by using the stepped doping design in collector to reduce the electric field between collector and sub-collector region under high current bias condition, known as the Kirk effect. Therefore, the collector epitaxial structures should be properly designed.

To reveal the ruggedness performance, the safe operating area (SOA) is often used for the device level evaluation. The wider SOA can be obtained by proper epitaxial design, device layout and process optimization, which are all the keys to improve ruggedness. According to the literatures, single emitter or small size device such as 5 μm^2 [2], 3 μm x 8 μm x 1 finger [3], 3.2 μm x 3.0 μm x 1 finger [4] are often utilized to demonstrate the SOA. However, the multi-finger device as unit-cell is a more common method for power cell combination for power amplifier. Therefore, if we purely apply the idea of collector design of small device for multi-finger device, the effectiveness will be lower than what is expected. It is due to the thermal coupling effect exhibiting

an extremely non-uniform current distribution on multi-finger device. In this paper, the study for evaluating the device ruggedness performance through experimental verification is presented. The study results show the improvement in SOA by implementing the optimal collector doping profile. Furthermore, after evaluating the device-level dc and SOA characteristics, the RF and power performances are revealed as well.

EPITAXIAL DESIGN AND SOA MEASUREMENT

To ensure acceptable base-collector breakdown voltage, a lowly doped collector is designed for the off-state (zero current) breakdown. However, it degrades the breakdown voltage at very high currents. To tackle this problem, the non-uniform or stepped doping between the base region and sub-collector region have been proposed [3, 5]. Sufficiently large SOA can be achieved at both low and high current operations simultaneously. In this work, two-steps doping concentration design for the collector layer is used with its doping being lower near the base and higher near the sub-collector. However, the thickness and doping concentration of the collector have significant influence not only on breakdown characteristics, but also on RF performance. The highly doped collector portion degrades the breakdown voltage at low collector current and also causes the degradation of RF performance by high base-collector capacitance. The lowly doped collector portion leads to the increase of the on-resistance and the decrease of cut-off frequency.

The SOA test involves sweeping the collector voltage with constant base current input and monitoring the breakdown voltage. The main purpose is to be able to compare and monitor various epitaxial structures at high and low current density operations. First, the measurement of small emitter size devices is performed. In the Fig. 1, two 4 μm^2 emitter-size devices with different collector profiles are selected for SOA measurement. The structure-A was designed with optimized two-steps collector. In the I_c - V_{ce} plane, the SOA curve was defined by the breakdown loci that induce the device fail. As seen, the structure-A demonstrates significant SOA improvement (> 3 V) over the baseline structure at all current operations.

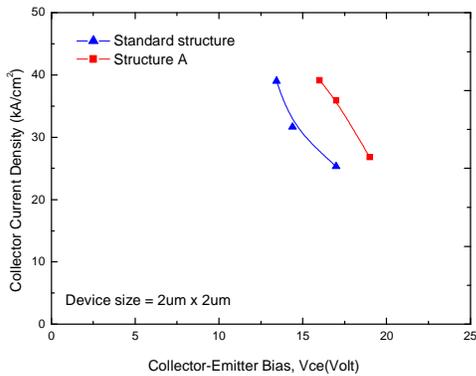


Fig. 1 The SOA results of optimized epi Structure A which was designed and measured by small size device.

THERMAL COUPLING EFFECT AND BREAKDOWN ANALYSIS

In practical application, the multi-finger type of HBTs is often used for the power amplifier. Therefore, a “large” emitter size of 3 $\mu\text{m} \times 40 \mu\text{m} \times 3$ fingers with the structure-A and baseline structure were used for SOA measurements. The measured results with large emitter-size are showed in Fig. 2. As we can see, there is no significant improvement in structure-A. The reason for this discrepancy is that there is the thermal couple effect caused by self-heating when the device is operated at high power condition. Therefore, both the self-heating effect and the breakdown effect for multi-finger devices should be considered in the epitaxial design.

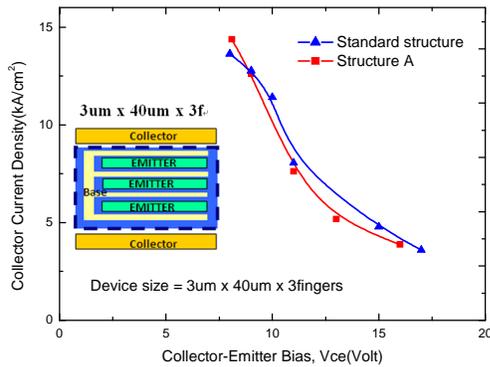


Fig. 2 The SOA results of Structure A measured in large size device. It shows that SOA has no improvement for Structure A.

In order to know the thermal couple effect in multi-finger devices, we designed a test structure for monitoring the individual finger current of multi-finger device.

Fig. 3 shows the collector current of each finger with I_b at 300 μA . For layout symmetry, only one of the two outer fingers is shown in Fig. 3. It is worthwhile to note two interesting points from the Fig. 3. Firstly, the center finger

handles more current density when the power level is increased. It is revealed that the high junction temperature of center finger can be obtained by thermal couple effect so that the effective potential barrier is reduced and conducted more collector current density. Secondly, it can be observed that the device failed occurs at the outer finger at this current density.

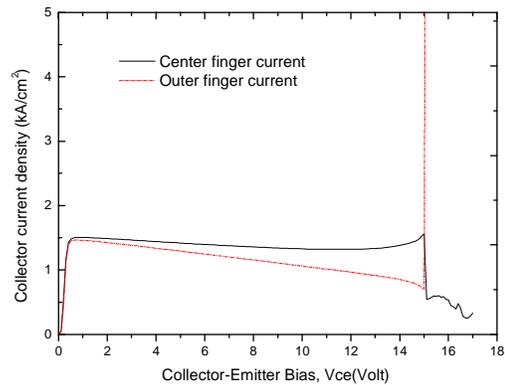


Fig. 3 Measured individual collector currents of three fingers while the input base current was fixed at 300 μA . The solid lines and dashed lines are the data measured from the center and the outer fingers.

However, when we increased the base current, the breakdown location is not at the outer finger but at the center finger, which is shown in Fig. 4. It indicated that the breakdown location for multi-finger device depends on the bias condition and current density. It is due to the non-uniform current distribution which induces the different electric field loci at different bias conditions. For small-device, the Kirk-effect is the dominate factor. Therefore, looking at small device SOA performance is not sufficient to reflect it in real application.

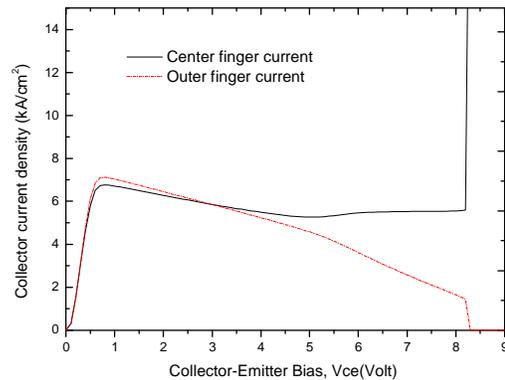


Fig. 4 Measured individual collector currents while the input base current was fixed at 1.2 mA.

In order to further investigate the mechanism, the two-dimensional (2-D) semiconductor simulation package SILVACO was employed. The HBT cross-section for simulation is shown in Fig. 5. A concentration dependent Analytic mobility model was included in the simulation to approximate the effect of doping on the mobility of electrons and holes in the material. Due to the high base doping concentration, Bandgap Narrowing model is included in base layer. Recombination mechanisms are approximated by concentration dependent Shockley-Read-Hall, and Auger recombination models [6]. In order to simulate the breakdown voltage and the effect of the impact ionization, the Selberherr's Model should be implemented as well. Thermal effects are considered in the simulations with thermodynamic model.

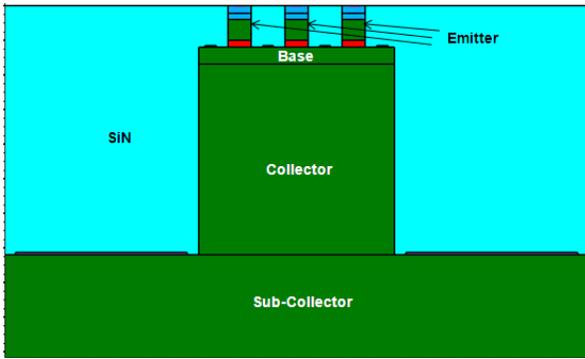


Fig. 5 Device structure of the 3 fingers HBT.

The simulated electric field and impact-generation rate characteristic of the low current operation are shown in Fig. 6. The bias condition in this simulation is the same as the bias condition in Fig. 3. The simulation result shows that the maximum impact-generation rate occurs at the base-collector interface underneath the outer finger. The impact ionization effect is a pure generation process and depends on the electric field and the current density. The rate is written as

$$G = \alpha_n \cdot \frac{|J_n|}{q} + \alpha_p \cdot \frac{|J_p|}{q} \quad (1)$$

where α_n and α_p are the electron and hole ionization rates, respectively. The electron ionization rate α_n can be written by

$$\alpha_n = \alpha_n^\infty \cdot \exp\left(-\left(\frac{E_n^{crit}}{E}\right)^{\beta_n}\right) \quad (2)$$

where α_n^∞ , E_n^{crit} , and β_n are constants that depend on semiconductor material and magnitude of the electric field. From equations (1) and (2), high electric field and high current could accelerate impact-ionization breakdown. Fig. 6 shows that the highest electric field is beneath the outer

fingers and leads to the avalanche breakdown eventually. In opposite, when the device operates at high current density, the electric field at base-collector interface is lower due to the Kirk effect. Fig. 7 illustrates the contour of electric field, current density, and impact-generation rate at high current operation (same bias condition as Fig. 4). In contrast with the contours in Fig.6, the maximum impact-generation rate is beneath the center finger even though the electric field at outer finger is maximal. This is due to a severe thermal coupling effect between these three fingers while the center finger begins current conducting from the nearby fingers. Therefore, the high current induces the high impact-ionization rate.

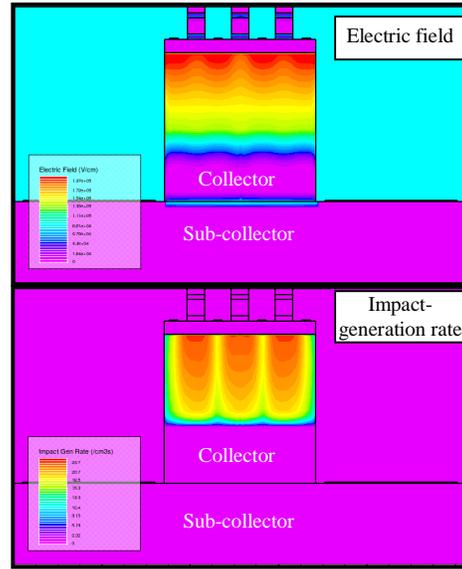


Fig. 6 The simulated electric field and impact-generation rate for low current operation.

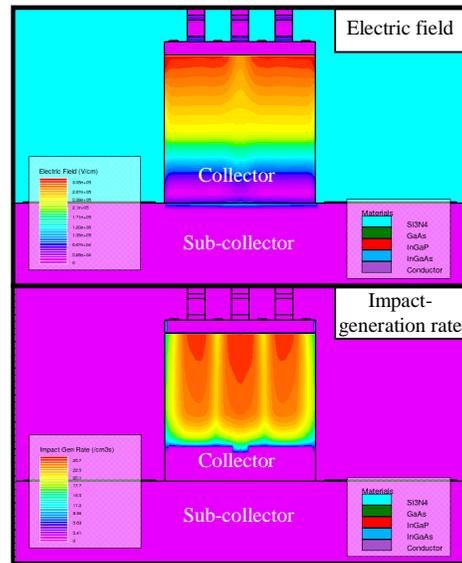


Fig. 7 The simulated electric field and impact-generation rate for high current operation.

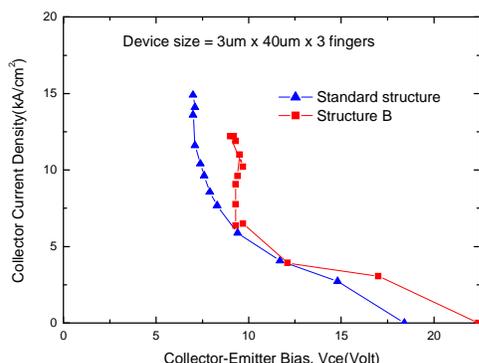


Fig. 8 The SOA comparison for standard structure and Structure B devices

In order to overcome the electrothermal issue, the structure-A was modified and optimized as the revised structure-B based on the experiment measurements and TCAD simulations. Fig. 8 clearly shows that the structure-B effectively improve the SOA with aforementioned thermal behavior of multi-finger HBTs. The power test was performed for the multi-cell HBT with total emitter size of $5760 \text{ } \mu\text{m}^2$. The operating frequency is 900 MHz and the quiescent current was set as 100 mA at VCE of 3.6 V. The experimental results are summarized in Table I. The P1dB and gain in structure-B are higher than that of the baseline structure. This degradation of fT is mainly caused by the increase in the collector thickness. These results indicate that the structure-B has outstanding RF and power performance. This new structure also has passed WIN's customer ruggedness qualification and is ready for mass-production

TABLE I
THE SUMMARIZED DC AND RF CHARACTERISTICS OF STANDARD STRUCTURE AND STRUCTURE B DEVICES

DC/RF Parameters	Standard structure	Structure-B
Beta	76.0	73.2
BK_BC	30.5 (V)	37.4 (V)
BK_EC	14.1 (V)	17.2 (V)
f_{max} @ $V_c = 3.6\text{V}$, $J_c = 25\text{kA/cm}^2$	111.7 (GHz)	112.4 (GHz)
f_T @ $V_c = 3.6\text{V}$, $J_c = 25\text{kA/cm}^2$	31.4 (GHz)	27.8 (GHz)
Power Performance	Standard structure	Structure-B
P1dB	24.68 (dBm)	28.02(dBm)
Gain	13.38(dB)	16.44(dB)
$P_{\text{out, sat}}$	28.29(dBm)	29.28(dBm)

CONCLUSIONS

The investigation and optimization of the epitaxial design for high ruggedness performance are presented. The SOA measurement by using small emitter size device is not a

suitable approach for the ruggedness evaluation due to the neglecting of thermal effect. In this paper, we use large device for SOA measurement and analyze the breakdown behavior by individual finger current monitoring. To understand the mechanism, TCAD simulator is used for the electric field, impact-generation rate analysis, and epitaxial optimization. Based on the DC, RF, and power measurement results, the structure-B is a good candidate for high ruggedness applications.

REFERENCES

- [1] D. Hill, et al., *28V thermal-impedance HBT with 20W cw output power*, IEEE Trans. Microwave Theory and Tech., vol. 45, pp.2224, 1997.
- [2] Cristian Cismaru, et al., *High Volume Test Methodology for HBT Device Ruggedness Characterization*, 2010 GaAs MANTECH Technical Digest, pp.65-68, May 2004.
- [3] Chien-Ping Lee, et al., *The Safe Operating Area of GaAs-Based Heterojunction Bipolar Transistors*, IEEE Trans. Electron Devices, vol. 53, no. 11, pp. 2681-2688, Nov. 2006.
- [4] M. Pfost et al., *Optimization of the collector profile of InGaP/GaAs HBTs for increased robustness*, IEEE GaAs Digest, pp.115-118, 2003.
- [5] T. Niwa et al., *A composite-collector InGaP/GaAs HBT with high ruggedness for GSM power amplifiers*, IEEE MTT-S Digest, pp.711-714, 2003
- [6] T. Tauqeer, et al., *Two-Dimensional Physical and Numerical Modelling of InP-based Heterojunction Bipolar Transistors*, International Conference on ASDAM 2008, pp. 271-274, Oct. 2008