Evaluation of Existing GaAs MIM-Capacitor Processes for Use with High-Voltage GaN MMIC Technologies

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Abstract

In this paper several existing industrial GaAs MIM-capacitor processes were evaluated regarding their suitability for use with high-voltage GaN MMIC technologies. These processes were tested using different time domain voltage stress methods from which lifetime estimations based on the linear field model were calculated. In addition the influence of electrode geometries and dielectric thicknesses on capacitor performance was investigated. Furthermore early device failures were correlated with defects detected on MIM bottom electrodes, these defects being identified by automated inspection methods.

INTRODUCTION

Metal-Insulator-Metal (MIM)-capacitors are important building-blocks for the realization of Monolithic Microwave Integrated Circuits (MMICs) based upon both GaAs and GaN technologies. As the requirements regarding device operational voltages are significantly higher for GaN compared to GaAs, a thorough assessment of any existing GaAs MIM process is required before its use in a GaN-based MMIC component can be contemplated.

At UMS a variety of PECVD-based MIM-capacitor processes for use in the production of GaAs MMICs exist. These processes all utilize silicon nitride (SiN) as the insulating material, since it is easy to deposit and its properties are well known. Furthermore it is possible to control the properties of the deposited SiN-film, by varying deposition parameters such as plasma-power, gas-flow, pressure and temperature.

Due to the comparatively low bias voltages of GaAs MMICs, associated MIM-processes are typically qualified for maximum operation voltages up to 30 V. For GaN MMICs, where DC bias voltages in the region of 30 V and above are employed, AC voltages of 90 V or more may occur across the MIM-elements due to resonant circuit effects. As such, MIM-capacitors as used in GaAs processes might not offer sufficient reliability performance for use with a high-voltage GaN MMIC technology and therefore an assessment of their applicability is required.

EXPERIMENTAL

The basic structure of the tested MIM-devices is shown in Figure 1. The tested structures were mainly processed on resistive GaAs substrates with 400 nm thick layer of highly insulating SiN deposited on the unprocessed wafer surface. This serves as an isolation layer between any subsequently deposited layers and the substrate itself. This was necessary, in order to eliminate the effects of parasitic leakage current flow through the substrate. In the realized test structures, the bottom capacitor electrode (Metal 1) had a thickness of 2.5 µm and consisted of a Ti/Pt/Au metal stack as with the standard GaAs MIM process. The desired MIM SiN dielectric layer was then deposited, whereby various SiN types and thicknesses were utilized. Finally the top electrode, 7 µm of Au (Metal 2), was formed through electroplating.

Different MIM-geometries (square, circular and octagonal) and pad areas between $8x10^{-4}$ mm² and $4x10^{-2}$ mm² were realized.

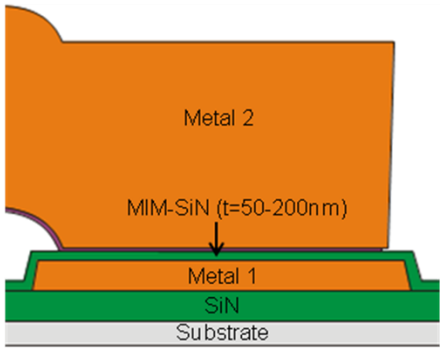

Figure 1: MIM-Structure, as used in this investigation.

Three nitrides, with nominally the same refractive index have been investigated:

1. MIM nitride A, processed in a multi wafer PECVD tool,
2. MIM nitride B, processed in a single wafer PECVD tool at temperatures slightly higher than the deposition temperature of MIM-nitride A,
3. MIM nitride C, which was supplied by an external research department, deposited in an ICPECVD tool at a lower temperature than nitrides A and B.

For testing the properties of the specific MIM-nitrides a ramped voltage method [1] was chosen, since it is possible to

accurately determine early device failures in short time periods [2]. Ramps of 4 V/sec (fast), 0.4 V/sec (medium) and 0.04 V/sec (slow) were utilized. The ramps were implemented as staircase voltage waveforms where the steps were adjusted to achieve the desired ramp-rate (e.g. 1 V step in 0.25 sec for the 4 V/sec ramp). All measurements were carried out using a HP4155A parameter analyzer in combination with a semiautomatic Cascade probe station and Metrics ICS software.

To estimate the lifetimes of the respective SiN dielectric layer the linear field model suggested by Cramer [2] was utilized. According to Slater [3] the time to failure, TTF, can be determined using the following expression:

$$TTF = t(0)\cdot\exp[\gamma(E_F - E_A)] \qquad (1)$$

where:

$$t(0) = \frac{\Delta t}{1-\exp(-\gamma\Delta E)} \qquad (2)$$

Here γ is an acceleration factor, which can be determined graphically by comparing the electrical field at failure of at least two different voltage ramps, E_F is the breakdown field, E_A is the applied field, Δt is the ramp step time and ΔE is the field step due to the ramp.

Results And Discussion

In order to understand the basic behavior of the tested SiN dielectric layers, I-V characteristics including destructive breakdown of 15 geometrically identical MIM devices for each SiN type have been recorded. These characteristics can be seen in Figure 2. In each case, the SiN dielectric thickness was 150 nm, the pad area was 126x126 µm² and the ramp-rate was 0.4 V/sec. The curves for other ramp-rates show similar characteristics, albeit with a shift in breakdown voltage, which will be addressed later in this paper.

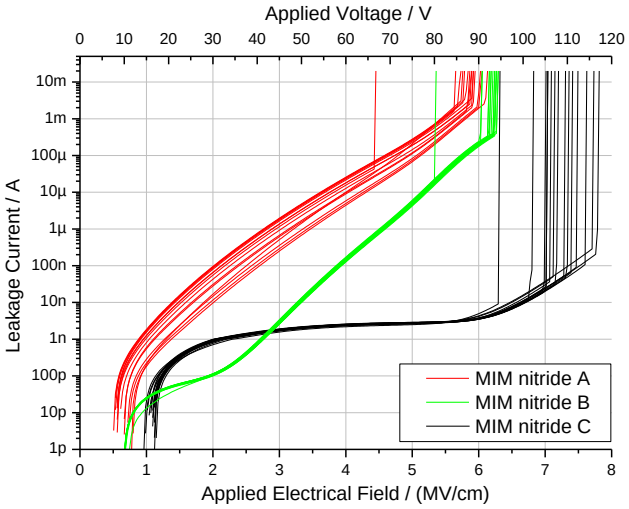

Figure 2: IV-characteristics of the different SiN types.

As can be seen in Figure 2, the three nitrides exhibit quite different leakage current and breakdown behaviors. MIM nitride A shows the highest leakage current, the lowest breakdown field and the widest spread in the I-V characteristics. The MIM dielectric layer B has an approximately two orders of magnitude lower leakage current than MIM nitride A for applied fields below 4 MV/cm. Furthermore there is lower spread visible and the breakdown occurs very homogeneously between 90 V and 95 V. MIM nitride C exhibits the lowest leakage current of all three SiN types, however, the breakdown voltage shows the largest spread in the range of about 1.5 MV/cm.
With respect to the devolution of the single I-V characteristics of the different SiN layers there appears to be only one conduction mechanism in MIM nitride A (probably the Frenkel-Poole mechanism) while in the MIM dielectric layers B and C at least two mechanisms are visible (for low applied fields the ohmic mechanism and for high fields the Frenkel-Poole mechanism).

The influence of circular, octagonal and square pad geometries on device performance has also been investigated. Here 30 MIM devices with the SiN dielectric layer B with a thickness of 150 nm and a pad area of $4x10^{-2}$ mm² were tested with the slow (0.04 V/sec) and the medium (0.4 V/sec) ramp-rate up to destructive breakdown – the results being shown in Figure 3. Here, early device failures have not been included since their origin lies in defects on the bottom electrode or in the SiN dielectric layer independent of the device geometry.

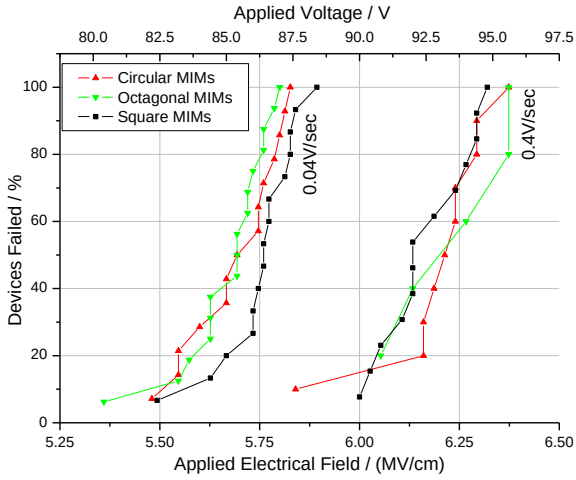

Figure 3: Distribution of failures for different geometries.

As shown in Figure 3, the failure distributions associated with the different geometries are equal. As such, we can state that the device geometry did not have a significant effect on the breakdown behavior of the SiN dielectric for the tested geometries and therefore would not be assessed in any of the remaining tests.

Since the target capacitance density (pF/mm²) for the GaN MMIC technology at UMS has not been defined and thinner layers are always desirable regarding processing time and

film uniformity, the influence of the thickness of the nitride comes into focus. For that reason a SiN dielectric layer, which has been developed at UMS and is comparable to MIM nitride C in regards of the conduction mechanisms and the leakage current level, was deposited with thicknesses of 50 nm, 100 nm, 150 nm and 200 nm. Then, 15 MIMs with a pad area of $4x10^{-2}$ mm² were tested for each thickness with the medium ramp (0.4 V/sec) up to destruction.

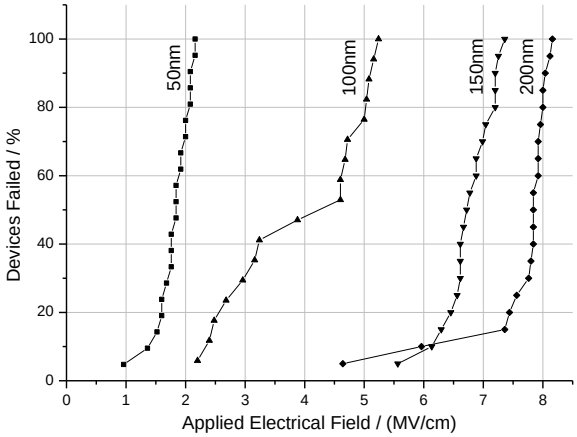

Figure 4: Failure distribution for different nitride thicknesses.

As seen in Figure 4, an interesting observation has been made that the normalized breakdown electric-field strength is proportional to the dielectric thicknesses. Below a thickness of 150 nm the breakdown field of the MIMs is unacceptably low (below 5 MV/cm) and the spread in the breakdown field is particularly high for the 100 nm thick nitride.

According to [4] a possible reason for this low breakdown field might be the increased inhomogeneous dielectric thicknesses for thinnest dielectric layers. These defect areas might be caused by micro-in-homogeneities, particle or metal residues. Another reason might be the surface roughness of the underlying electrode (Metal 1) layer. In Figure 5 an atomic force microscope (AFM) image of an area of 1 µm² of the 2.5 µm thick bottom electrode layer is shown.

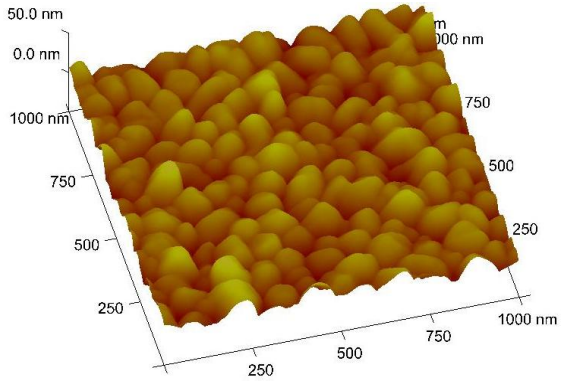

Figure 5: AFM record of the bottom electrode of the MIM structure.

Surface roughness analysis of this sample yields a root mean square value of 6.4 nm and a maximum peak-to-valley value (R_{max}) of 44.7 nm. As such, if the peak and the valley point lie close to each other, there might be localized height differences as high as 44.7 nm. If the nitride is deposited over this step it will not have a uniform thickness and as a consequence the electrical field might be significantly higher, this resulting in premature MIM breakdown. This phenomenon might explain the low breakdown voltages for thicknesses below 150 nm, since its effect is more pronounced for thinner dielectrics.

To investigate the other defect sources which can cause localized SiN thinning, the bottom electrode layer was scanned with a KLA 2135 automatic optical inspection (AOI) tool before the desired SiN dielectric was deposited. Typically 5 % of the 500 scanned bottom electrodes per wafer were affected with specific defect types - these being shown in Figure 6.

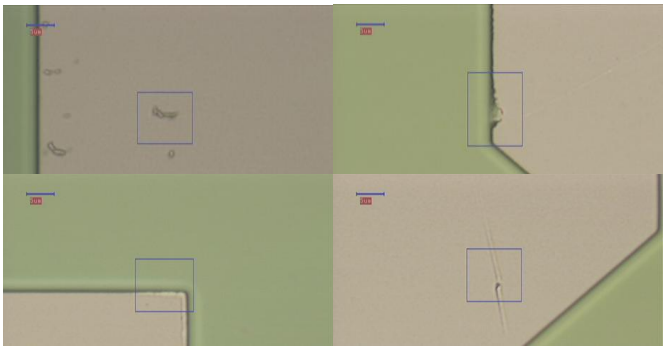

Figure 6: Typical defects found on the bottom electrode, from top left clockwise: lift-off metal residues; edge breaking, scratches, resist residues

A statistical analysis reveals that the defects were situated mainly on the bottom electrode of the inspected devices with larger pad areas ($2.4\text{-}4x10^{-2}$ mm²). The identified defects can be grouped into lift-off metal residues, edge breaking, resist residues and scratches due to poor handling procedures or non optimum tool parameters.

MIM structures with various device geometries and identified defects were tested to destruction using a 0.4 V/sec voltage ramp.

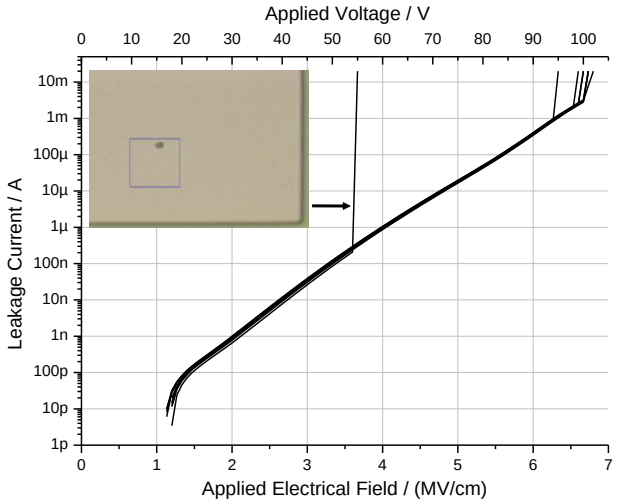

Figure 7: IV-characteristics of $4x10^{-2}$ mm² big MIMs with homogeneous breakdown; one early failure is visible.

In Figure 7 the IV-characteristics of MIMs with the largest pad area of $4x10^{-2}$ mm² are shown. Here a rather homogeneous breakdown field is visible, despite one early failure. The inset shows the AOI scan (taken prior to the deposition of the SiN dielectric) of the bottom electrode of the MIM structure which showed the early failure. Here one metal residue (comparable to top left picture in Figure 6) is clearly visible, being responsible for early breakdown during testing – the point of breakdown was correlated with the AOI detected defect through FIB crossection analysis.

Since temperature acceleration plays only a minor role for MIM failure [2] an operational lifetime estimation has been carried out at room temperature. Therefore, MIMs with relatively small pad areas (126x126 µm²) have been chosen to rule out the increased possibility of undesired early extrinsic failures due to the types of defects reported previously. In Figure 8 the failure distributions of MIM devices with MIM nitride B and a thickness of 150 nm for the different ramps are shown. It can be seen that for the fast ramp the intrinsic breakdown field lies significantly higher than for the slow ramp. This correlates well with the proposed intrinsic breakdown mechanism given in [4].

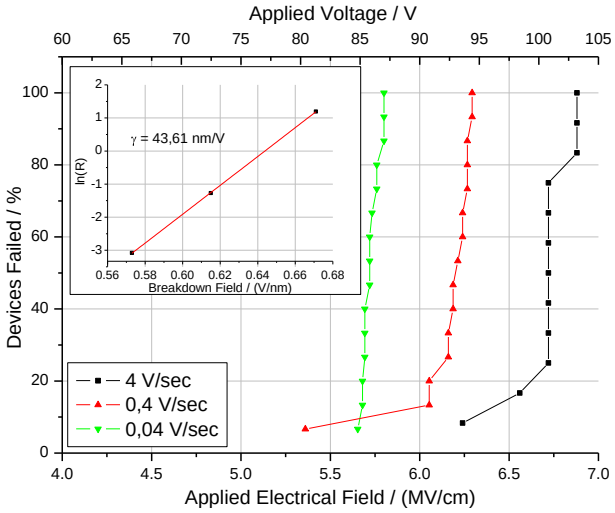

Figure 8: Failure distribution of MIM nitride B for different ramp rates; the inset plot shows the corresponding determination of the acceleration factor.

For the extraction of the acceleration factor γ, the median breakdown field (the applied electric field whereby 50 % of the devices have failed) is extracted and plotted against the natural logarithm of the utilized ramp rates, as shown in the inset plot of Figure 8. The linear fit of this plot yields an acceleration factor of 43.6 nm/V for the MIM structures with MIM nitride B and acceleration factors of 29.8 nm/V and 28.1 nm/V for MIM nitrides A and C respectively. These values correspond well with previously reported values [2, 3].

From the determined acceleration factors and the use of the formulas (1) and (2) it is now possible to estimate the lifetime for the different nitrides for operation at 30 V. In Figure 9 the extrapolated lifetimes for the three evaluated nitride types in addition to the target lifetime of 20 years are shown. It can be seen that only the MIM structures with the SiN dielectric B are able to achieve a target lifetime of 20 years. The MIM structures with other nitride types lie below the desired minimum lifetime thresholds. Increasing the thickness of the SiN dielectric would result in an increase in estimated lifetime for all nitride types, since the thickness plays an important role as shown previously.

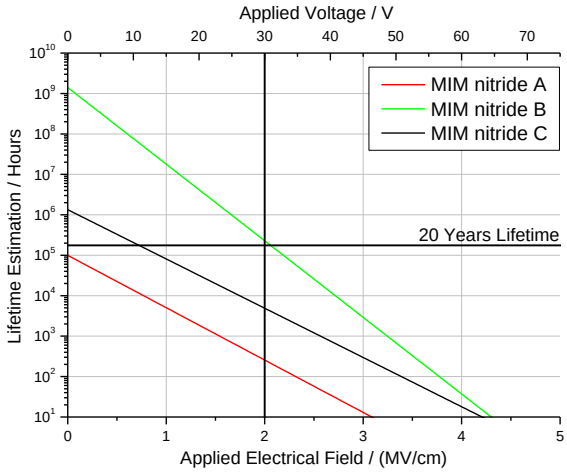

Figure 9: Lifetime estimation for the different nitrides; only MIM nitride B is able to deliver 20 years of lifetime.

Conclusion

In this paper existing GaAs MIM-capacitor processes have been evaluated regarding their suitability for use with high-voltage GaN technology. Three SiN dielectric types have been tested regarding their electrical performance and it has been shown that that the MIM nitride thickness has a strong influence on the breakdown behavior for a normalized electric field strength, while the geometry of the MIM-pad does not play a major role. Furthermore, defects on the bottom electrodes of tested structures were investigated with the help of an AOI tool and early MIM breakdown was correlated with metal lift-off defects. Finally lifetime estimations for all three nitrides were carried out, which showed that one of the available MIM capacitor processes currently used in GaAs MMIC technologies at UMS is a promising candidate for use in a high-voltage GaN MMIC technology.

Acknowledgements

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