TCAD Modeling and Simulation of a Field Plated GaN MOSFET for High Voltage Applications

K. Bothe[1], M. Johnson[2], D. Barlage[1]

[1]Department of Electrical Engineering, University of Alberta, Edmonton, Canada
kbothe@ualberta.ca, barlage@ualberta.ca, (780) 492-4081
[2]Department of Materials Science and Engineering, University of North Carolina, Raleigh, USA

Keywords: GaN MOSFET, High Breakdown Voltage, Power MOSFETS

Abstract

We have modelled a normally-off GaN MOSFET that has enhanced device characteristics over leading GaN HFET devices used in power electronics. The structures and dimensions of the GaN-based device were all achieved through simulation optimization. Our modeled device shows a maximum current density of 1.2 A/mm with an on-resistance of 6.15 Ω*mm. Including field plate structures sustained the MOSFET to a breakdown field of 400 V/um.

INTRODUCTION

Switching based semiconductor devices are critical components found in many industrial and consumer electrical power systems, including power inverters in hybrid electric vehicles and power switches and generators for electrical grids [1-2]. Based on the simulated results we believe the optimized GaN MOSFET will improve the breakdown voltage and leakage current compared to present GaN HFET technology.

We examine the effects that shape, size and field plates have on its device characteristics of a GaN MOSFET. Materials used for power semiconductor devices are compared through Baliga's Figure of Merit (BFOM) [3]. The BFOM shows that there are advantages to use GaN (*BFOM = 868*) over traditional Si (*BFOM = 1*) technology. However, to reach the maximum performance, we will show that the GaN MOSFET is a more ideal option. Current HFET approaches have difficulty in achieving the project results because of a non-ideal off state.

SIMULATION AND MODELING

To model the device characteristics of a GaN MOSFET, we used Synopsys Sentaurus TCAD. Through simulations we can predict the characteristics and behaviour of the devices. Parameters are consistent with values found from many research groups [4-7]. To create the best performing device we optimized the body thickness, channel length and gate-drain length. Furthermore, we examined the common technique that includes field plates on the gate and source to increase the breakdown voltage of the device [8].

Figure 1 illustrates the GaN MOSFET structure and the variables used to determine the optimized and enhanced GaN MOSFET. To ensure that the GaN channel was in the

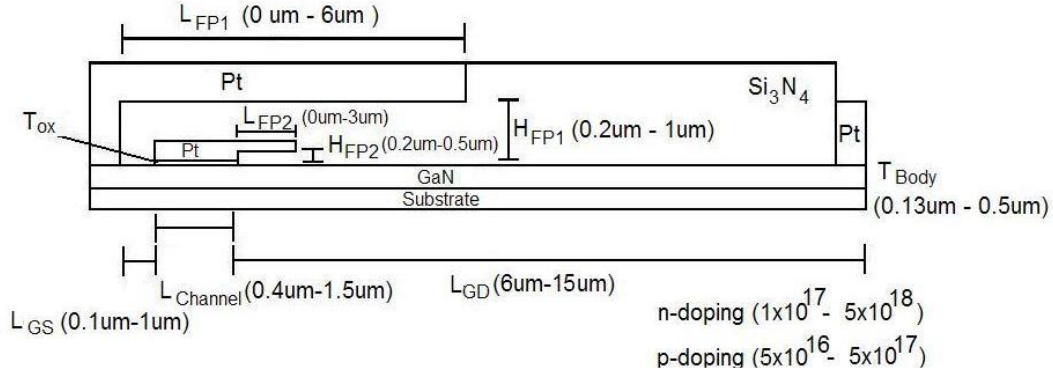

Figure 1: This is the structural design of the GaN MOSFET, where the variables were optimized. The values indicate the ranges that variables were simulated.

depletion region, simulations found that the body thickness was required to be one-third of the gate length. The optimal channel length that maintained a large breakdown voltage without degrading the current density was 1.2 um, shown in Figure 2. This provided a starting point to increase the complexity of the design. By including the source and gate field plates, the breakdown voltage improved while maintaining the current density and reducing the slope of the saturation region.

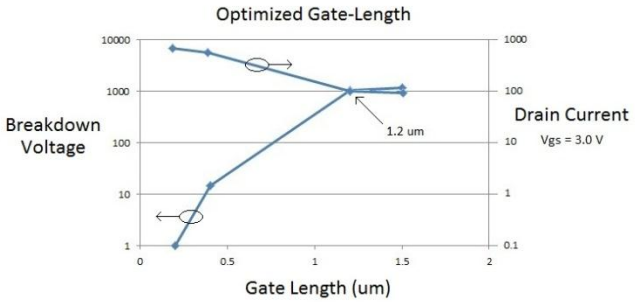

Figure 2: (a) The family of curves for a 12um gate-drain length.

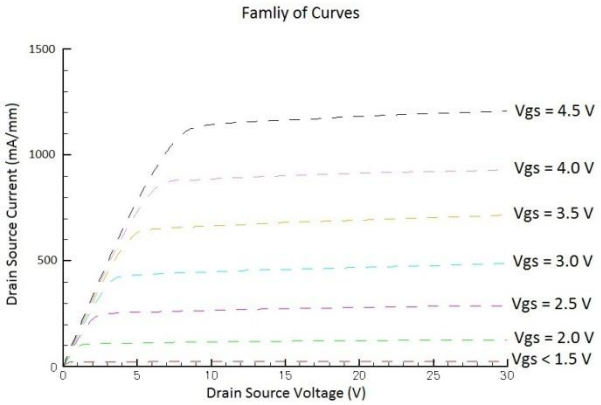

Figure 3: The family of curves for a 12um drain length.

The family of curves and breakdown voltage for a 12um gate-drain length is shown in Figure 3 and Figure 4. The gate voltage was only simulated up to 4.5 V because we accounted for potential dielectric breakdown after 5 V in the gate oxide. The 12 um gate-drain length device was simulated and determined to have a peak current density of 1.2 A/mm with an on-resistance of 6.15 Ω*mm. Additionally, the field plates suppressed the electric field, pushing the breakdown field to 400 V/um. This resulted in a device breakdown voltage of 4800 V where the drain leakage was < 5 uA/mm. The capacitance evaluation from the simulated results (see Figure 5) confirms that the threshold voltage was 1 V for a 6 um device however; the threshold voltage changed to a maximum of 1.5 V as the gate-drain length was increased.

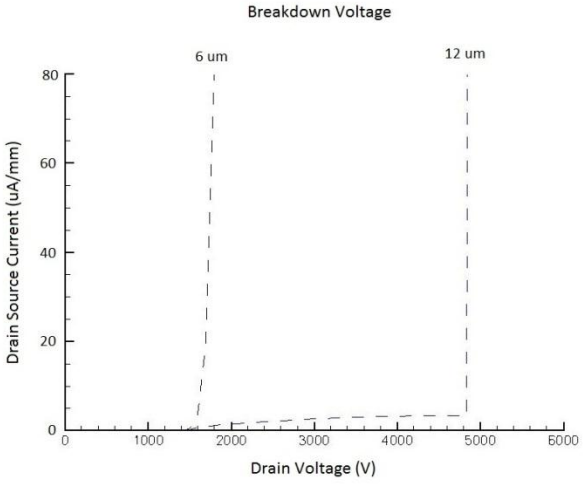

Figure 4: The breakdown with the addition of a gate and source field plate.

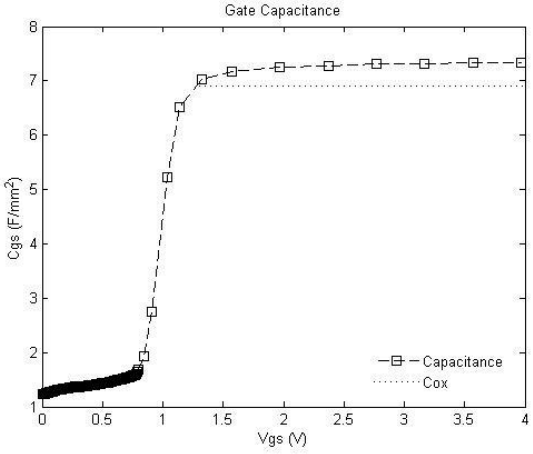

Figure 5: The gate-source capacitance of a 6um drain length MOSFET with a Cox = 6.9 nF/mm^2.

Following the design of the MOSFET, we created a modelled version of a current HFET design built by HRL Labs [10] as shown in Figure 6. The dimensions and structures were systematically altered to recreate the physical device. From these simulations we were able to examine the device characteristics of the HFET and compare the results to our optimized MOSFET design. Our simulated HFET recreated similar family of curves and breakdown voltages for equivalent device dimensions.

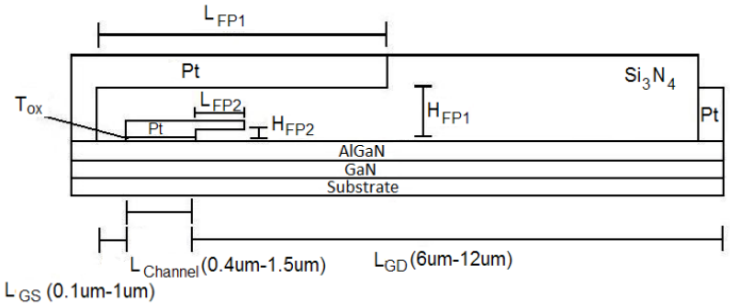

Figure 6: The structural design of the GaN HFET

When comparing the HFET to the MOSFET, we determined that the 6 um gate-drain length (L_{GD}) MOSFET could produce the equivalent current density as the 8 um HFET while maintaining a much larger breakdown voltage. We believe the cause of a lower breakdown voltage is due to the minimum carrier concentration in the device. The MOSFET has a much lower minimum carrier concentration than the HFET. This will reduce the avalanche breakdown effect in a MOSFET, whereas the HFET will begin to breakdown prematurely due to the latent excess carriers in the channel.

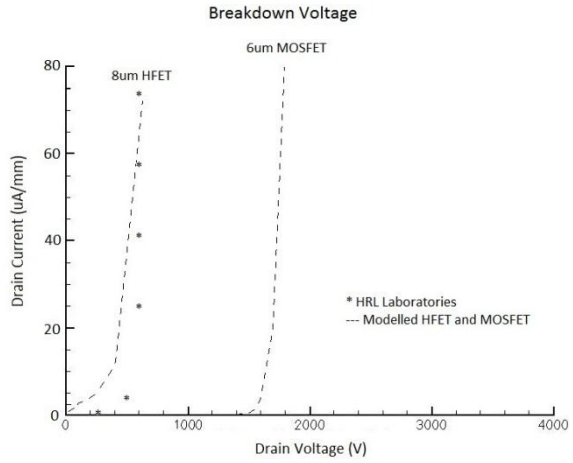

Figure 7: The comparison between breakdown voltage of the modeled HFET and current HFET technology [10].

The results from the simulations above have shown that a normally-off GaN MOSFET will produce a large current density and breakdown voltage with a low leakage current. When comparing this device to current HFET technology, the GaN MOSFET the lower carrier concentration in the off state leads to less opportunities for avalanching and a subsequently higher break-down voltage. Furthermore the thinner gate dielectric allows the GaN MOSFET to have greater control of the channel electric field compared to the HFET device (see Figure 8). Because of the superior carrier control, the optimized GaN MOSFET is capable of preventing a breakdown voltage no less than 2.5 times larger than the HFET. In addition, the maximum simulated gate voltage of the MOSFET was restricted by the potential catastrophic dielectric breakdown, unlike the HFET which was restricted by current collapse phenomena [9]. With improved gate dielectrics, the GaN MOSFET gate voltage can maintain larger values; thus, producing even a substantially larger current density than our conservative estimates.

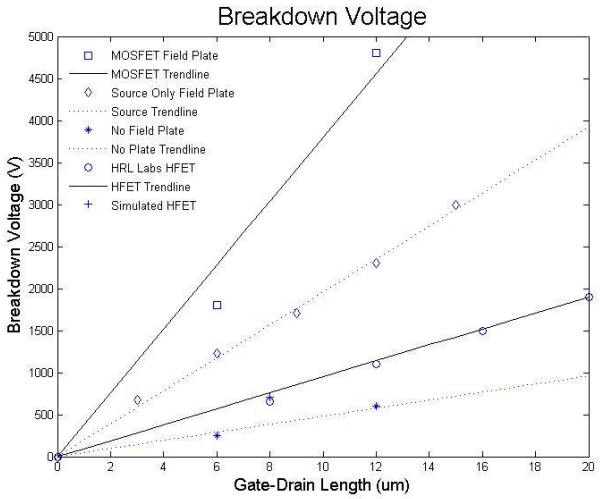

Figure 8: The comparison between breakdown voltage of the modeled GaN MOSFET and current HFET technology [10, 11].

CONCLUSION

Through optimization of the GaN MOSFET we have determined the dimensions and structures required to obtain a device with peak performance. This design is capable of handling larger breakdown voltages as well as lower current leakage. Due to the lower minimum carrier concentration, the GaN MOSFET is able to have reduced dimensions, while still maintaining a much larger breakdown voltage than the HFET. The modelled normally-off GaN MOSFET has shown that terminal device characteristics are potentially significantly enhanced over the GaN HFET. The difference in device architecture provides multiple opportunities to enhance the efficiency and reach the maximum power handling capabilities of GaN based electronics.

ACKNOWLEDGEMENTS

National Science Engineering and Research Discovery Program, and the University of Alberta Electrical and Computer Engineering Department.

REFERENCES

[1] M. Amin and J. Stringer, "The electric power grid: today and tomorrow," MRS Bull., **33** (2008) 399

[2] A. Raskin and S. Shan, "The Emergence of Hybrid Vehicles", Alliance Bernstein, Research on Strategic Change, (2006)

[3] B. J. Baliga, "Power Semiconductor Device Figure of Merit for High-Frequency Applications" IEEE Electron Device Letters **10** (1989) pg. 455

[4] J. Kim, M., et al. "Delta-doping of Si in GaN by Metalorganic Chemical Vapour Deposition", Japanese Journal of Applied Physics, **38** Issue 2A, (1999), pg. 681

[5] C. Bayram, et al. "Delta-Doping optimization for high quality p-type GaN" Journal of Applied Physics, **104** Issue 8, (2008) pg. 83512

[6] J. Park, A. Ozbek, et al. "Analytical model of source injection for N-type enhancement mode GaN-based Schottky source/drain MOSFET" Solid State Electronics, **54** Issue 12 (2009), pg. 1680

[7] W. Huang, T. Khan, T.P. Chow, "Comparison of MOS Capacitors on n- and p- type GaN" Journal of Electronic Materials, **35** Issue 4 (2006) pg. 726

[8] R. Trew and U. Mishra "Gate breakdown in MESFETs and HEMTs" IEEE electron Dev. Lett., **12**, (1991) pg. 524

[9] W. Saito, et al. "High-Voltage GaN-HEMTs for power electronics applications and current collapse phenomena under high applied voltage", CS MANTECH Conference, May 14-17, (2007) pg. 209

[10] K.S. Boutros, et al. "Normally-off 5A/1100V GaN-on-silicon device for high voltage applications", IEDM IEEE International (2009) pg 161

[11] Y. Uemoto, et al. "GaN monolithic inverter IC using normally-off gate injection transistors with planar isolation on Si substrate"IEDM IEEE International (2009) pg. 165

ACRONYMS

GaN: Gallium Nitride
HFET: High Electron Mobility Transistor
MOSFET: Metal Oxide Field Effect Transistor
BFOM: Baliga's Figure of Merit