Self-Aligned $In_{0.53}Ga_{0.47}As$/InAs/InP Vertical Tunnel FETs

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Abstract

A relatively simple and self-aligned vertical tunneling field-effect transistor (VTFET) process has been demonstrated using $In_{0.53}Ga_{0.47}As$/InAs/InP heterojunctions. At 300 K, the VTFETs show an on-current of 3 – 4.8 μA/μm and a minimum subthreshold swing (SS) of 220 mV/dec using Al_2O_3 gate oxide. The corresponding tunneling diodes exhibit negative differential resistance under forward bias over a range of temperatures, which confirms that the conduction mechanism is indeed band-to-band tunneling. This new self-aligned process is attractive to quickly realize and test VTFET designs.

INTRODUCTION

Tunnel field-effect transistors (TFETs) are under intense investigation for low-power applications because of their potential for extremely low subthreshold swing and low off-state leakage [1]. However, most of the efforts in the literature have been focused on Si-and Ge-based TFETs, which exhibited a low on-current (I_{on}) due to the high tunneling barrier and effective mass [2-4].

III-V semiconductors with small effective mass and broken band lineup are considered to be ideal for TFETs in that they promise high on-current and I_{on}/I_{off} ratios. Especially, heterostructures with type-II or -III band alignment represent the narrowest possible *p-n* junctions. Type-II band alignment has also been investigated as TFET performance boosters in the Si/SiGe heterosystem [5-7]. However, the best way to realize compound-semiconductor-based TFETs is still an open question, given the processing constraints in comparison with Si. It is challenging to achieve planar *p-n* junctions with sharp lateral doping profiles; on the other hand, precise control of the band diagram can be realized in an epitaxial growth, but placement of the gate and excessive parasitic capacitances may be issues in vertical FETs. So far, only a few reports have been published on the experimental demonstrations of III–V TFETs. For instance, in Ref. [8] $In_{0.53}Ga_{0.47}As$ TFETs using 10-nm Al_2O_3 gate oxide with a saturation current of 20 μA/μm (V_{GS} = 2 V) and an *SS* > 150 mV/dec were demonstrated for the first time. In Ref. [9] an improved on-current of 50 μA/μm (V_{GS} = 2 V) and a minimum subthreshold swing (SS) of 86 mV/dec were achieved by using 5 nm atomic-layer-deposited HfO_2 gate oxide and $In_{0.7}Ga_{0.3}As$ tunnel junctions.

In this paper, we report for the first time a self-aligned and potentially manufacturable vertical TFET process demonstrated using an $In_{0.53}Ga_{0.47}As$/InAs/InP pocket vertical heterojunction. Pocket vertical TFETs are adopted in this study since in these structures the gate electric field can augment the internal tunnel junction electrical field, thus more effectively control the band overlap for minimal subthreshold swing [10]. An I_{on}/I_{off} ratio of 10^4 and I_{on} of 3 – 4.8 μA/μm with SS of 220 mV/dec at 300 K have been achieved. These results are largely limited by the unoptimized ohmic contacts, interface density of states under the gate, and traps in the tunneling junction. We also investigated the effects of temperature variation on the device performance of tunnel FET and tunnel diodes to confirm the physical mechanism underlying the observed device operation.

DEVICE STRUCTURE AND FABRICATION

Fig. 1 shows a cross sectional schematic diagram of the N-channel $In_{0.53}Ga_{0.47}As$/InAs/InP vertical TFET that has been fabricated. A gate-first self-aligned process was used to minimize drain access resistance. The TFETs were grown by molecular beam epitaxy (MBE) on a *p*+ InP substrate (Zn ~ 1.7 x 10^{18} cm^{-3}). The device structure comprises 300 nm of *p*+ InP and 12 nm of *p*+ InP (Be ~ 1.2 x 10^{19} cm^{-3}), followed by 2 nm of *n*+ InAs and 13 nm of *n*+ $In_xGa_{1-x}As$, with the In composition *x* graded from 1.0 to 0.53. The n+ layers are Si doped, to a concentration of 1 x 10^{19} cm^{-3}.

Fabrication processing started with atomic layer deposition (ALD) of an 8 nm thick Al_2O_3 gate dielectric, followed by a blanket deposition of a Ti/W/SiN_x gate stack.

It is necessary to remove the *p*+ InP under the drain contacts and the insulating spacer to turn off the TFETs. To this end, we studied the vertical and lateral etching characteristics of InP using an $HCl:H_3PO_4$ (1:3) solution, which is selective to InAs and $In_{0.53}Ga_{0.47}As$. Patterns along various crystal directions were made using Shipley 1813

positive photoresist and optical lithography. After selective etching of $In_{0.53}Ga_{0.47}As$ and InAs using H_2SO_4:H_2O_2:H_2O (1:8:160) solution and InP using HCl:H_3PO_4 (1:3) solution, photoresist was removed by acetone and cross sections were inspected in a scanning electron microscope (SEM). Fig. 2 shows that the InP etch rate along [001] and [010] crystal directions is much higher than that along [011] and $[01\bar{1}]$ directions (no undercut), consistent with the observations reported previously [11]. It is thus concluded that the edges of the rectangular TFETs need to be aligned parallel to <001> directions to ensure uniform underetch of InP.

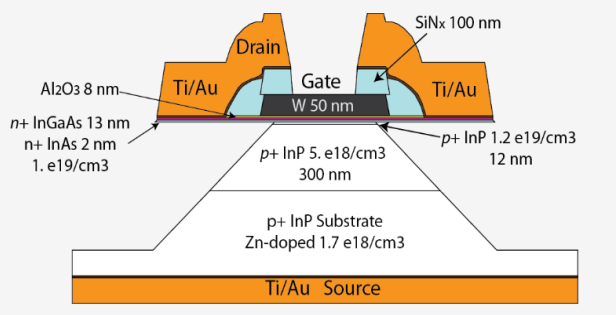
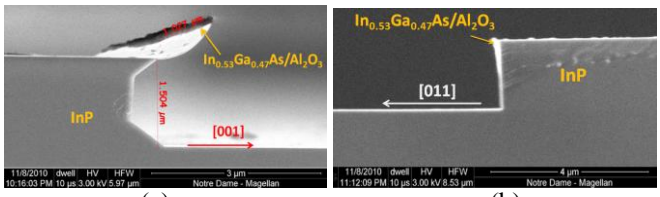


Fig. 1. Cross section of a vertical $In_{0.53}Ga_{0.47}As$/InAs/InP TFET fabricated using a gate first self-aligned process.



(a) (b)

Fig. 2. Cross section of InP profile after etching with mask aligned perpendicular (a) to [001] showing significant InP undercut and (b) to [011] showing negligible InP undercut or etch.

The Ti/W/SiN_x gate stack was patterned using optical lithography and reactive ion etching (RIE) with mask aligned parallel to [001] and [010] directions. Plasma-enhanced chemical vapor deposition (PECVD) SiN_x sidewalls were then formed around the gate stack by blanket deposition and anisotropic dry etch, followed by removal of Al_2O_3 gate dielectric using AZ400K developer as a selective wet etchant. After Ti/Au source metallization (on the back of the wafer) and drain metallization and liftoff (Ti/Au), $In_{0.53}Ga_{0.47}As$ and InAs were selectively etched by H_2SO_4:H_2O_2:H_2O (1:8:160) solution. SiN_x in the gate stack was etched by RIE to expose the gate metal (Ti/W), followed by a highly selective InP etch using HCl:H_3PO_4 (1:3) solution until the InP under the drain and the SiN_x spacer was removed, forming the undercut mesa structure. Finally, the device was passivated with 7 nm of Al_2O_3 and 3 nm of HfO_2, deposited using ALD at 300 °C.

Shown in Fig. 3 are the cross sectional images of a fabricated $In_{0.53}Ga_{0.47}As$/InAs/InP vertical TFET, taken on a Helios NanoLab DualBeam 600 focused ion beam (FIB)/SEM system. From the SEM images, we observed that InP has been etched laterally for 1.45 µm, while the drain length is about 736 nm and the SiN_x spacer is about 150 nm thick. The SEM images clearly indicate that the current modulation observed in these $In_{0.53}Ga_{0.47}As$/InAs/InP tunnel junctions is entirely due to the gate control.

These devices were tested at room temperature using an Agilent 1500B semiconductor parameter analyzer on a Cascade 11000 probe station with microchamber. The temperature-dependent measurement was performed using a Lakeshore cryogenic probe station with a Keithley 4200 semiconductor characterization system.

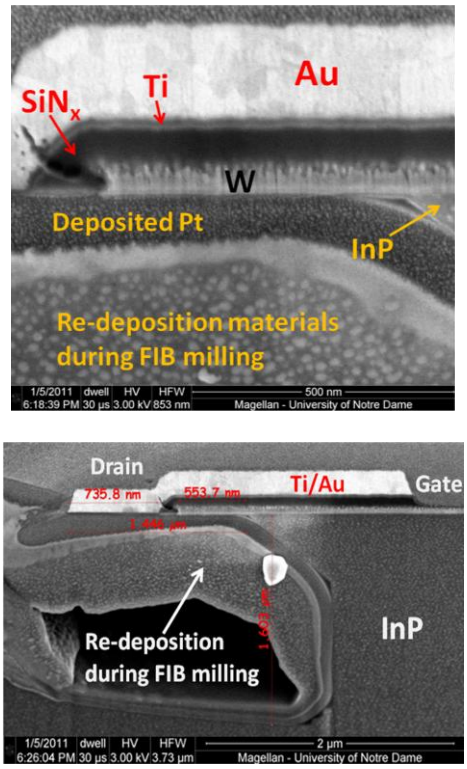


Fig. 3. FIB/SEM cross sections of a fabricated vertical $In_{0.53}Ga_{0.47}As$/InAs/InP TFET: (upper) featuring SiN_x sidewall and InP undercut etch, and (lower) a lower-magnification view of the self-aligned drain contact and device structure after etching in HCl:H_3PO_4 (1:3).

Results and Discussion

Fig. 4 shows the measured I_d-V_{ds} characteristics of an $In_{0.53}Ga_{0.47}As$/InAs/InP TFET while stepping the gate voltage from -1 to 1 V at 300 K. The top gate dimension was designed to be 50 x 80 µm^2. As expected, we observed that VTFETs can only be turned off if the InP mesa is sufficiently undercut along all four edges of the mesa. Due to unintentional misalignment during processing, typical

VTFETs normally have the device current dominated by one edge, where the field is highest. Based on this understanding, we note that the transistor shown in Fig. 4 has an on-current at V_{GS} =1 V of 3 – 4.8 μA/μm depending on whether the measured current is normalized to 80 or 50 μm gate width (since it is not clear a priori which edge will have the dominant current). This is close to the expected value for InP based TFETs. The smaller on current compared to the reported $In_{0.53}Ga_{0.47}As$ and $In_{0.7}Ga_{0.3}As$ TFETs is due to the larger bandgap of InP (1.34 eV) relative to InGaAs (E_G = 0.58 eV for $In_{0.7}Ga_{0.3}As$ and E_G = 0.73 eV for $In_{0.53}Ga_{0.47}As$).

Fig. 5 shows the measured I_D–V_{GS} transfer characteristics of a TFET at 300 K for V_{DS} = 0.5 V and 1 V. The minimum point subthreshold swing values of about 240 and 220 mV/dec were achieved at V_{DS} = 0.5 V and 1 V, respectively. The drain current on/off ratio is about 10^4, while the gate leakage is at least two orders of magnitude smaller than the device channel current.

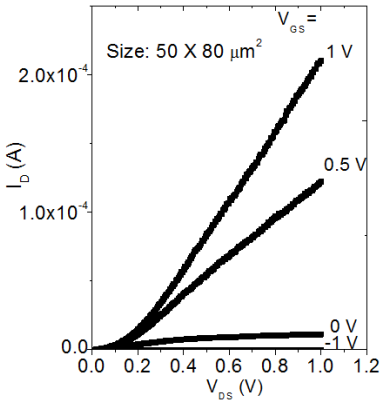


Fig. 4. I_D versus V_{DS} for gate voltage V_{GS} stepped from -1 to 1 V of a self-aligned $In_{0.53}Ga_{0.47}As$/InAs/InP VTFET at 300 K.

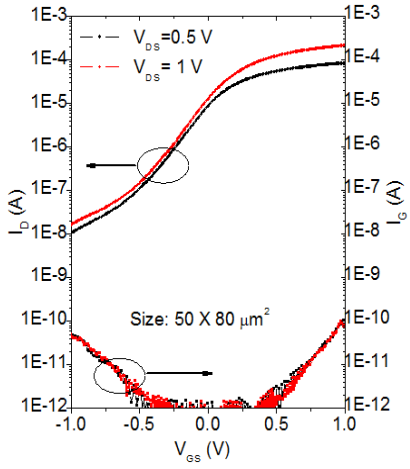


Fig. 5. Measured transfer curves and gate leakage current on a self-aligned $In_{0.53}Ga_{0.47}As$/InAs/InP VTFET at 300 K.

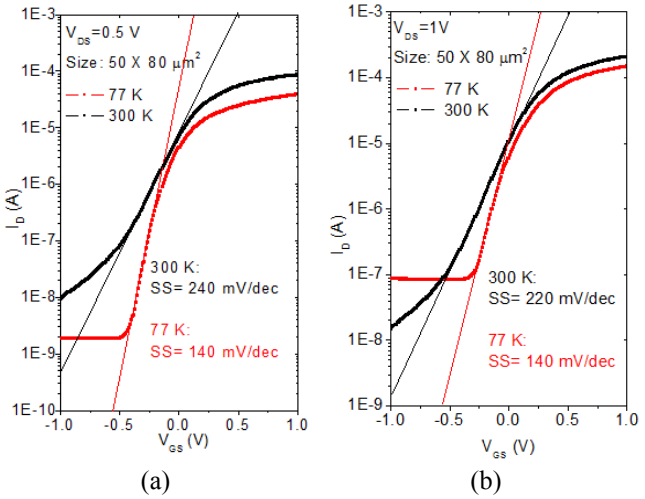


Fig. 6. Temperature dependent I_D–V_{GS} characteristics of a $In_{0.53}Ga_{0.47}As$/InAs/InP TFET. (a) At V_{ds}= 0.5 V, the minimum point subthreshold swing SS_{min} decreased from 240 mV/dec at 300 K to 140 mV/dec at 77 K; (b) at V_{DS} = 1 V SS_{min} decreased from 220 mV/dec at 300 K to 140 mV/dec at 77 K

The I_D–V_{GS} characteristics of the vertical TFETs were also measured at 77 K. As shown in Fig. 6, the drive current at 77 K is lower than that at 300 K, while the increased off-state current in Fig. 6(b) was due to accidental scratching of the sample by the probes, and is not indicative of intrinsic device performance. The minimum point subthreshold swing, SS_{MIN}, was found to improve at 77 K compared to that at room temperature, with a measured SS_{MIN} of 140 mV/dec for both V_{DS} = 0.5 V and 1 V being observed at 77 K. Since band-to-band tunneling has a relatively weak temperature dependence, the reduced drive current and improved SS_{MIN} at 77 K are attributed to the following mechanisms: 1) reduced interface trap response [8], 2) reduced trap-assisted tunneling, 3) increased bandgap, and 4) poor ohmic contact resistance at low temperatures in comparison to room temperature.

The drain current in a TFET's common-source *I-V* characteristic results from gate-modulation of the Zener tunneling current of the reverse-biased tunnel junction in the source (the drain is labeled so that V_{DS} is positive for the Zener tunneling condition). In order to confirm the band-to-band tunneling mechanism is responsible for the operation observed in our VTFETs, we measured the temperature dependent *I-V* characteristics of $In_{0.53}Ga_{0.47}As$/InAs/InP tunnel diodes fabricated on the same epitaxial structure. The results are shown in Fig. 7(a). Negative differential resistance (NDR) is clearly observed under negative V_{DS}, i.e. forward bias for the *p*+ InP/ *n*+ InAs / *n*+ $In_{0.53}Ga_{0.47}As$ tunnel junction. As shown in Fig. 7(b), both the peak and valley currents vary with temperature, with the trend that the currents increase with increasing temperature. This leads to

a reduced peak-to-valley current ratio at higher temperatures. These observations are consistent with the VTFET characteristics above. To improve device performance, further studies are necessary to reduce the density of trap states at the heterojunction and at the gate dielectric/ semiconductor interface, and improve the ohmic contacts.

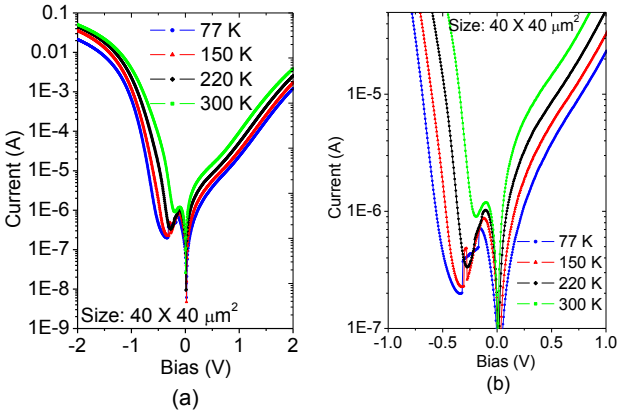


Fig. 7. (a) Representative current-voltage characteristics of the p+InP/n+InAs/n+$In_{0.53}Ga_{0.47}As$ tunnel junction for temperatures ranging from 77 to 300 K. (b) Expanded view of the temperature dependence in the current range about the NDR.

CONCLUSIONS

A simple and self-aligned vertical tunnel FET process using $In_{0.53}Ga_{0.47}As$/InAs/InP heterojunctions has been demonstrated for the first time. An I_{on}/I_{off} ratio of 10^4 and I_{on} of 3 - 4.8 μA/μm with SS of 220 mV/dec at 300 K have been achieved. The effects of temperature and traps on the VTFET performance and tunnel diodes were also investigated. Through improvements in interface state densities, reduced trap-assisted tunneling, and designs with low bandgap materials and favorable Type II or III band alignment, significantly enhanced TFET performance is expected in future devices. This new self-aligned process provides a promising approach for quickly fabricating and testing designs for III–V TFETs for ultralow-power digital applications.

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ACRONYMS

SEM: Scanning Electron Microscope
VTFET: Vertical Tunnel Field-Effect Transistor