Type-II DHBTs Microwave Characterization and Metallization Issues

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Abstract: A process issue of sub-micron heterojunction bipolar transistors fabrication is described. The metal short occurred during metallization of emitter contact and succeeding wet etch is a major failure mechanism. We present the designs of experiment to identify and solve the problem. The microwave and DC performance of sub-micron Type-II DHBTs is demonstrated.

INTRODUCTION

InP transistors have the highest cutoff frequencies of any current transistor technology. The extraordinary carrier transport properties of InP HEMT with 50nm gate length [1] and HBT with 12.5nm base thickness [2] to reach highest power gain cutoff frequency (f_{MAX}) and current gain cutoff frequency (f_T), respectively. In InP-HBTs development, vertical scaling of material has been used to reduce transit time. However, as depicted in Fig. 1, this scaling leads to decreasing breakdown voltages as material layers are scaled. The direct correlation between power gain cutoff frequencies and base-collector capacitance (C_{bc}) also explains the vertical scaling tradeoff between f_{MAX} and f_T. In order for balanced f_T/ f_{MAX} performance with high breakdown voltages which are required for mixed-signal sub-millimeter wave circuit designs, type-II InP/GaAsSb DHBT with InP collector has been shown to be able to achieve high speed and high breakdown voltage simultaneously [3]. The type-II DHBT has higher breakdown voltage for a given collector thickness than InP/InGaAs type-I DHBT and SHBT devices as shown in Fig. 2. The advantage of a type-II $GaAs_ySb_{1-y}$/InP band alignment over type-I InGaAs/InP DHBT is due to the fact that current blocking effect is eliminated at base/collector interface, enabling ballistic carrier injection into the collector to reduce collector layer transit time.

HBT FABRICATION PROCESS

The emitter contact is defined by 50 keV electron beam lithography using a bi-layer PMMA/PMGI photoresist stack. The Ti/Pt/Au deposition is done by electron beam evaporation and liftoff. After the emitter mesa etch, the self-aligned base ohmic contact is defined by EBL and Ti/Pt/Au electron beam evaporation. The base contact to emitter spacing is controlled by the timed wet etch. To self-align the base-collector mesa etch to the base contact edge, the active area is protected by a silicon nitride layer. The outside dimensions of the base contact width are varied from 550-1050 nm to control the base-resistance / base-collector capacitance tradeoff. This dimension is further controlled by the wet chemical etch undercut of the base-collector mesa etch. This completes the definition of the device active area.

The devices are completed by deposition of a collector contact on the sub-collector layer, re-aligned by EBL. A final post metal step is required to bring the base and collector contact pads even with the emitter post height. The transistors are then protected by a standard I-line photoresist during the isolation wet etch down to the semi-insulating substrate. The isolation etch removes the material between the active device and the base post pad, creating a base metal airbridge and eliminating parasistic C_{BC} associated with the pad. Following the isolation, the devices are planarized in

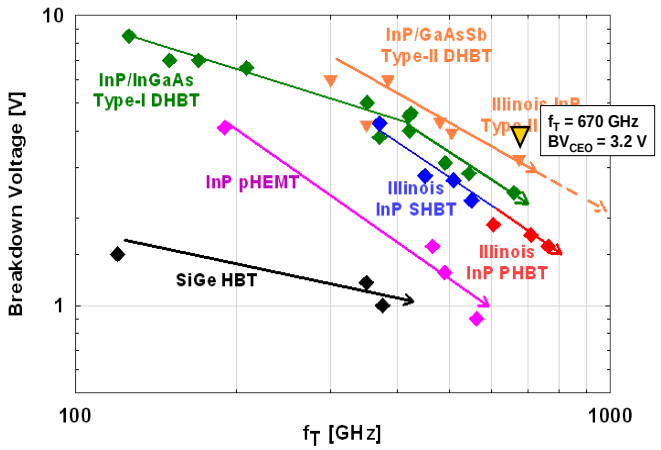

Figure 1. Breakdown voltage versus f_T scaling relationship of the various InP-based HBTs compared to InP pHEMTs and SiGe HBTs.

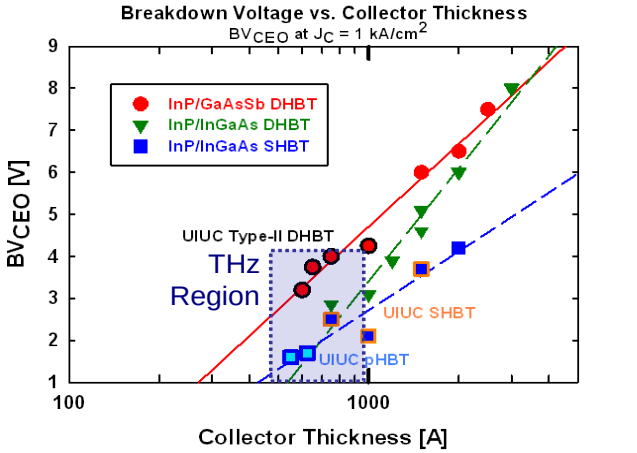

Figure 2. Reported off-state breakdown voltage versus collector layer thickness for InP SHBT/PHBT, type-I DHBT, and type-II DHBT. THz cutoff frequency devices will have collector layer thicknesses from 500 to 1000 Å.

BCB. The BCB is etched back by CF_4 RIE to expose the transistor contact posts.

Description Of Emitter Process Issues

As described in previous section, the emitter metal contact was defined by electron beam lithography. The photoresist is composed of a double layer stack with an electron beam sensitive top layer to define the pattern opening size and a bottom layer to create an overhang to facilitate the lift-off process. After development, a standard Ti/Pt/Au metal was deposited by ebeam evaporation. Even though the chamber is brought to high vacuum, each target metal in its vapor phase has enough kinetic energy to migrate freely on the surface of samples. Fig. 3 shows clearly the emitter metal spreading around the main emitter body. The succeeding step is the wet chemical etching to define the emitter mesa dimensions which utilized the emitter metal as the mask. After wet etching, the periphery of the emitter was surrounded by a thin "wing". The "wing" is a thin and porous metal. Because of the fact that base metal is self-aligned deposited, the undercut gap of emitter prevents emitter metal from shorting to base. If the wing is too long or too thick, it can collapse and impede further undercut etch, as shown in Fig. 4.

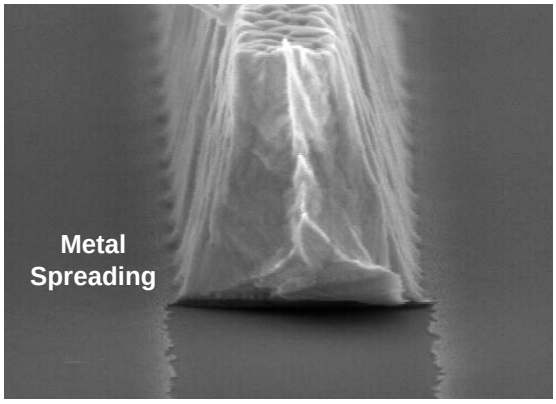

Figure 3. Breakdown voltage versus f_T scaling relationship of the various InP-based HBTs compared to InP pHEMTs and SiGe HBTs.

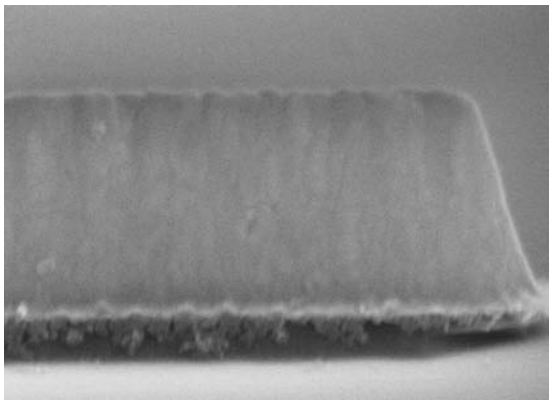

Figure 4. Emitter "wing" collapse after emitter mesa etch. The folded metal filament can cause emitter to base short.

Optimization Of Evaporator and Photolithography

One of the possible causes of the emitter wing is photoresist pull-back during evaporation. To eliminate the emitter shorting issue, we installed a thermal shield in the ebeam evaporator and optimize the ramping rate/time of each metal source. The temperature probe was used to measure the difference before and after the optimization work. Fig. 5 indicates that the thermal cycle has been reduced.

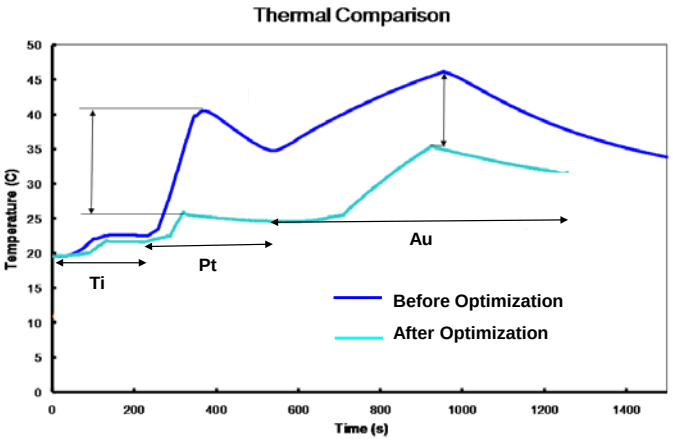

Figure 5. Thermal cycle comparison of ebeam evaporator optimization.

The other variable affecting wing size we discovered is the photoresist thickness and metal crucible size. The solid angle lines illustrate how these two factors affect metal spreading geometry (Fig. 6). By replacing a 1.25cm diameter gold crucible by a 0.5cm one, and reducing the bottom layer photoresist thickness, the wing size was finally reduced from 75nm to 25nm at each side of the emitter.

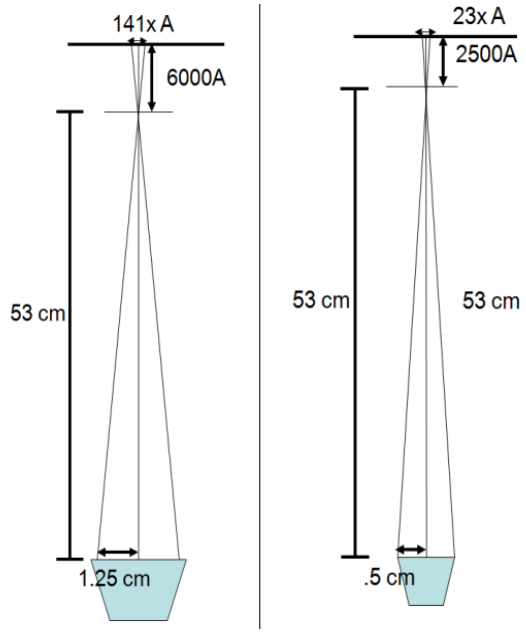

Figure 6. The crucible size and imaging resist thickness determine the emitter wing size by solid angle lines illustration.

MEASURED RF AND DC DATA OF SUBMICRON DHBTS

The graded base type-II DHBT was grown at University of Illinois using a gas-source MBE and the device structures presented in this work benefit from optimization of the compositionally-graded base growth conditions to facilitate higher carbon doping incorporation and high quality base-emitter interfaces. Sub-micron devices were fabricated with emitter widths as small as 300 nm and lengths ranging from 2 to 8 μm. Extrinsic parasitics are minimized using a self-aligned base-collector mesa etch with emitter sidewall spacer and by using an isolated base contact post. A device SEM image depicting these features is presented in Fig. 7. DHBT f_T performance was achieved by vertically scaling the base and collector epitaxial layers to 20nm and 60nm, respectively. Transistor S-parameters were measured from 0.5 to 50 GHz using an Agilent 8364B vector network analyzer. Off-wafer SOLT calibrations were used and measured on-wafer open and short probe pad parasitics were subsequently de-embedded from the measurements. A device with emitter area $0.3\times8\,\mu m^2$ has f_T = 680 GHz and simultaneous f_{MAX} = 175 GHz when operated at room temperature. The same device measured at -37ºC has simultaneous f_T = 745 GHz and f_{MAX} = 205 GHz at current density J_E = 8.3 mA/μm^2 (Fig. 8). DC characteristics of the device exhibit low offset voltage, small knee voltage progression, and 1kA/cm^2 BV_{CEO} = 3 V.

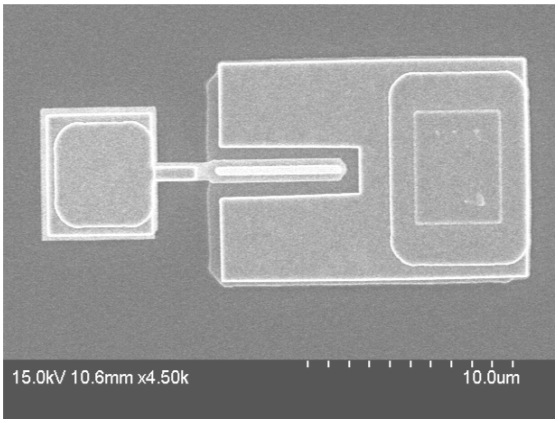

Figure 7. SEM of sub-micron HBT device (top view).

CONCLUSIONS

The submicron HBT process with optimized emitter contact metallization and self-aligned wet etch was demonstrated with sufficient yield for device-level research. The excellent cutoff frequency performance and high breakdown voltage shows great potential of Type-II DHBT in millimeter-wave integrated circuits application.

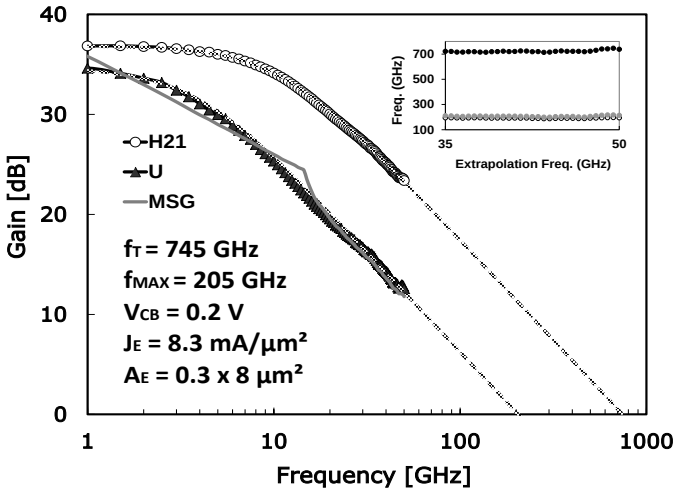

Figure 8. Measured RF data with extrapolations to f_T = 745 GHz and f_{MAX} = 205 GHz for device with A_E = 0.3x8 μm^2 on 20nm base, 60nm collector structure biased at -37ºC.

ACKNOWLEDGEMENTS

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ACRONYMS

BCB: bisbenzocyclobutene
DHBT: Double Heterojunction Bipolar Transistor
EBL: Electron Beam Lithography
HBT: Heterojunction Bipolar Transistor
f_T: Currrent gain cutoff frequency
f_{MAX}: Power gain cutoff frequency
RIE: Reactive-ion etching
SHBT: Single Heterojunction Bipolar Transistor
SOLT: Short-Open-Load-Through