110 GHz Characterization of Coplanar Waveguides on GaN-on-Si Substrates

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Abstract

We characterize the microwave loss in coplanar waveguides (CPWs) on AlGaN/GaN HEMT buffer layers on high-resistivity silicon (HR-Si) substrates, up to 110 GHz. To our knowledge, this is the first broadband characterization of CPWs on GaN-on-Si. Conventional CPWs on commercially available AlGaN/GaN on HR-Si HEMT layers show a loss as low as 0.8 dB/mm at 110 GHz. Losses are further reduced by etching trenches between the CPW conductors, reaching 0.47 dB/mm at 110 GHz. The work shows that CPWs on GaN-on-Si exhibit performances comparable to those built on S.I. InP, demonstrating the suitably of GaN-on-Si technology in mm-wave applications.

INTRODUCTION

Demand for high-power, high-frequency transistors for millimeter-wave systems operating at frequencies above 50 GHz is steadily increasing. New application domains such as indoor high-speed wireless links (short-range communication links which deliver 5 Gbit/s over 3-5 m at 60 GHz), and longer range line-of-sight systems delivering Ethernet-like performance (1-2 Gbit/s over 1 km at (71-76)/(81-86 GHz)) and in automotive radars (77 GHz). In order to become economically interesting, such systems require low-cost transistors which can deliver significant power levels at mm-wave frequencies. The wide energy gap ($E_G = 3.4$ eV) leading to high breakdown fields, the high saturated electron velocities ($v_S > 2\text{-}3 \times 10^7$ cm/s) and the high channel electron densities ($n_S \sim 10^{13}/\text{cm}^2$) found in GaN HEMTs enable the fabrication of devices which can handle large voltages and high current densities per unit size: in other words, GaN devices can deliver high power densities (in W/mm of unit transistor width) at both microwave and millimeter-wave frequencies.

The best GaN HEMT transistor performances have so far been achieved with epitaxial layers grown on SiC substrates. Unfortunately, the cost and ready availability of high-quality SiC semi-insulating substrates remain problematic for many organizations. In this context, GaN HEMTs on silicon were originally developed as a low-cost alternative to devices on SiC, which admittedly can handle somewhat lower power levels due to the lower thermal conductivity of Si substrates when compared to SiC. Recent work extended the frequency performance of AlGaN/GaN HEMTs grown on high-resistivity silicon (HR-Si) to previously unexpected levels [1-4], ultimately achieving cutoff frequencies exceeding 100 GHz in fully passivated 100 nm gate AlGaN/GaN HEMTs [5]. HR-Si substrates have also been successfully used with AlInN/GaN HEMTs, reaching cutoff frequencies as high as $f_T = 143$ GHz and $f_{MAX} = 176$ GHz, at a simultaneous bias point [6]. Such device performances naturally become interesting for millimeter-wave MMIC applications, but a thorough broadband characterization of substrate and/or buffer layer losses must first be carried out before a suitable mm-wave GaN-on-Si technology can evolve.

Circuit implementations naturally require interconnects and passive elements such as high-quality factor capacitors and inductors, as well as the ability to implement low-loss waveguides at mm-wave frequencies. The availability of low-loss transmission lines is then a key requirement for an AlGaN/GaN-on-Si MMIC technology. In the present work, we therefore characterize the broadband performance of coplanar waveguides (CPWs) built on commercially available AlGaN/GaN HEMT buffer layers grown on HR-Si, and report losses as low as 0.47 dB/mm at 110 GHz.

EXPERIMENTAL WORK

The coplanar waveguides were fabricated on commercially available standard AlGaN/GaN HEMT layers supplied by Nitronex Corporation [7]. The epitaxial layers are grown on 100 mm high-resistivity (10 kΩ-cm) float-zone refined (111) silicon substrates. The original layer stack (from the substrate up) consists of a transition layer, followed by an insulating GaN buffer and channel layer, an

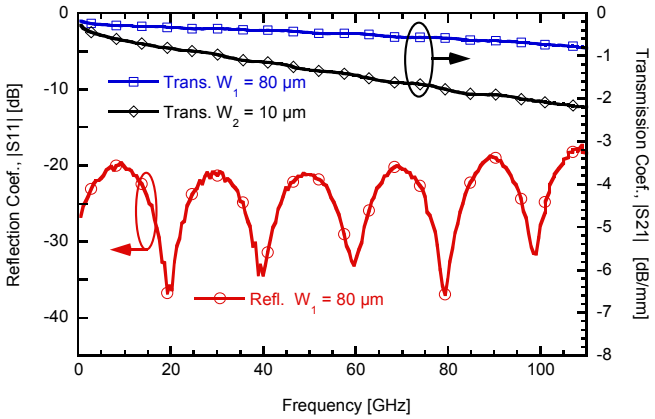

Figure 1. Reflection and transmission coefficients for 3-mm long CPWs with $W_1 = 80$ µm and $W_2 = 10$ µm center conductor widths. The attenuation at 110 GHz is ~0.8 dB/mm for the wide line and 2.2 dB/mm for the narrow line. The characteristic impedance of W_1 ~ 50 Ω over the full frequency range of interest, as evidenced by $|S_{11}| \approx -20$ dB.

18 nm $Al_{0.27}Ga_{0.73}N$ barrier and a 2 nm GaN cap. The transistor active region (the upper two layers) was etched away by ICP-RIE before the CPW fabrication. As in a standard MMIC process, the CPWs were deposited on the isolation mesa floor.

The first two transmission lines considered here consist of 3-mm long CPWs with respective center conductor widths $W_1 = 80$ µm and $W_2 = 10$ µm, and a 39 µm spacing to the 200 µm wide ground planes. The metallization stack consists of 50/100 nm evaporated Ti/Au followed by 1 µm of electroplated Au.

Our CPWs were characterized with a HP8510XF vector network analyzer (VNA) used to measure the *S*-parameters over the frequency range from 0.5 to 110 GHz. The VNA used a line-reflect-reflect-match (LRRM) calibration based on an off-chip impedance standard. Ground-Signal-Ground (GSG) Picoprobe probes were used for contacting the samples and the device under test was placed on a microwave absorber to minimize the effects of parasitic substrate modes. The measurement results are displayed in Fig. 1, showing that the CPW characteristic impedance is

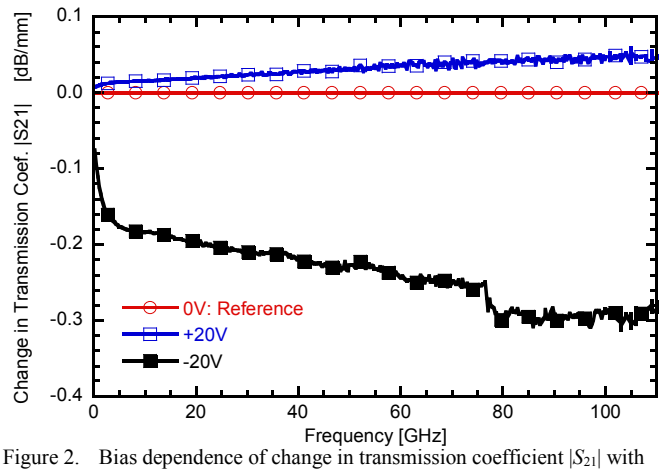

Figure 2. Bias dependence of change in transmission coefficient $|S_{21}|$ with applied potential between the metallization and wafer prober chuck for the low-loss structure with the 80 µm wide centre conductor.

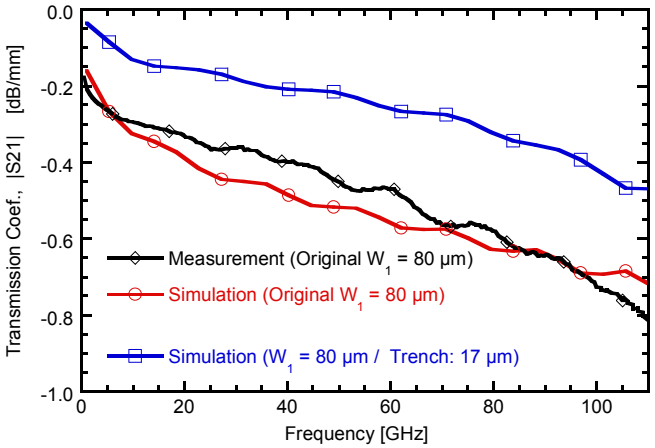

Figure 3. Comparison between measurement and simulation of the CPW with 80 µm center conductor and simulation of an optimized structure with trenches between the metallization.

very nearly equal to 50 Ω over the full band, as evidenced by the low input reflection coefficient $S_{11} < -20$ dB over the full frequency range. The attenuation on the wide line is only 0.8 dB/mm at 110 GHz. The narrow CPW shows a higher loss of ~2.2 dB/mm because of higher conductor losses and features a clear $\sqrt{f}$ skin effect frequency dependence.

The bias dependence of CPW loss was studied by applying a voltage between metallization and the wafer prober chuck (microwave absorber removed) through bias-tees. Varying the value and polarity of the bias influences the transmission line characteristics. This is shown below in Fig. 2 for the structure with the wide centre conductor. The results reveal parasitic *p*-type conduction under the CPW: positive biases repel positively charged holes and reduce the CPW loss, while negative biases have the opposite effect. During the growth of the nitride transition layer on the HR-Si substrate, the in-diffusion of aluminum and/or gallium atoms into the substrate leads to the formation a parasitic *p*-type doped silicon layer near the GaN/Si interface which can be significantly reduced by optimizing the growth conditions [8]. Silicon could also potentially act as a donor in the GaN buffer layers, but the results of Fig. 2 clearly show that the dominant loss mechanism occurs through *p*-type conduction.

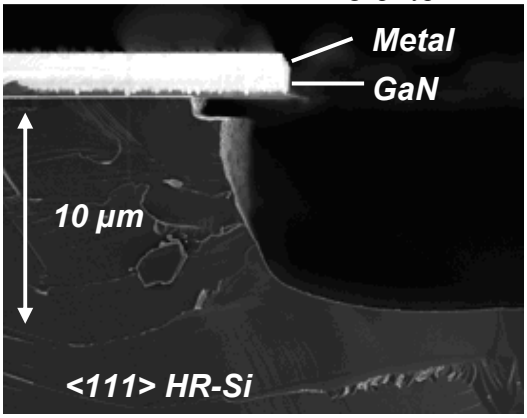

Figure 4. Scanning electron micrograph (SEM) image of cleaved CPW transmission line showing the trench between the center conductor and the ground planes. The trench depth was approximately 10 µm.

Using the above results as a starting point, we have sought to support the further optimization of our CPWs through numerical simulations with the 3D full-wave tool Ansoft HFSS. A model was first set up for the implemented CPWs, and the unknown parameters (effective relative dielectric constant of the transition layer, and conductivity of the parasitic *p*-type doped layer due to Al/Ga in-diffusion into the Si substrate) were adjusted to fit the measurement data of Fig. 3. The fitted conductivity of the parasitic *p*-layer, using the reported measured carrier distribution [8] was found to be about 8 S/m, a reasonable value for the measured hole density profile versus depth into GaN-overgrown Si (with a peak free hole concentration $p < 10^{16}$ cm^{-3}). The conductivity value is consistent with what is expected for *p*-type Si for similar doping levels [9]. The relative dielectric constant of the transition layer was set to 9, which is also sensible for AlGaN based materials. The resulting match between measurement and simulation is better than 0.1 dB/mm over the frequency range from 0.5 to 110 GHz. In a second step, this model was used to guide CPW optimization. The simulations showed that the line losses could be reduced by eliminating the conductive material between the metal traces, because the CPW electromagnetic field is concentrated in this space. Fig. 3 suggests that an improvement of 0.2-0.3 dB/mm could be achieved at high frequencies by defining 17 µm deep trenches between the conductor traces.

A second batch of CPWs was fabricated to experimentally determine the effects of trenching on the performance of our CPWs. For the trenched CPWs, different dimensions were chosen in order to keep the characteristic impedance of the lines at 50 Ω. The center conductor width was kept equal to $W_1 = 80$ µm, but the separation to the ground planes increased to 45 µm. Besides of the 200 µm ground plane width used in the first batch, structures with 75 µm wide ground planes were also processed. The metallization thickness was reduced to 25/750 nm evaporated Ni/Au. The GaN buffer layers were etched between the CPW conductors by ICP-RIE, all the way to the silicon substrate. The silicon substrate was then anisotropically wet etched in tetramethylammonium hydroxide (TMAH), which also undercut some 2 µm of silicon material under the CPW conductors. The silicon trenching procedure was concluded with ICP-RIE dry etching in O_2 and SF_6 process gases. Fig. 4 shows the resulting SEM cross-section of the trenched CPW transmission line.

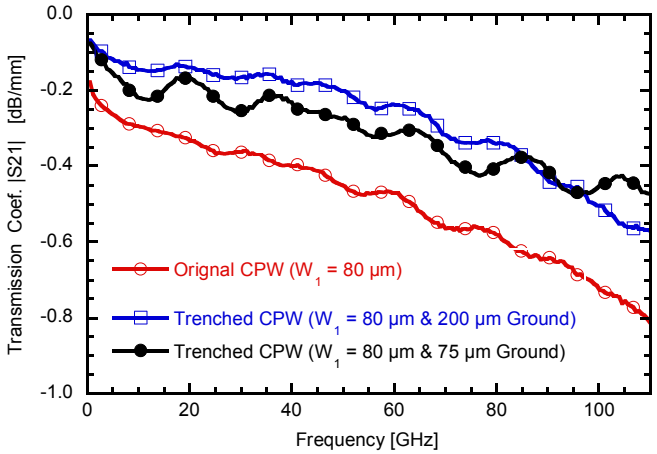

Figure 5. Measured transmission coefficient of CPW with an 80 µm wide center conductor, showing the original design, and two trenched designs with 200 and 75 µm ground plane widths. The trench etch depth was approximately 10 µm.

As depicted in Fig. 5, the resulting trenched CPWs indeed feature reduced losses of 0.47 and 0.57 dB/mm at 110 GHz, in excellent agreement with the simulations of Fig. 3. The structure with the narrower ground plane shows slightly lower losses towards higher frequencies (above approximately 85 GHz) due to coupling to parasitic modes, which is more pronounced for wider ground planes [10]. The crossover is explained by considering that the higher conductor loss in the narrower ground planes dominates at low frequencies, until radiation loss into the substrate eventually takes over at higher frequencies. The lower overall CPW attenuation measured at high frequencies with the narrow ground planes is owed to the considerably weaker radiation losses generated by narrower CPW ground planes [11].

CONCLUSIONS

We have characterized the broadband performance of CPWs implemented on commercial AlGaN/GaN HEMT buffer layers grown on HR-Si. At 60 (110) GHz losses of 0.47 (0.81), 0.24 (0.57) and 0.31 (0.47) dB/mm are obtained. These results are comparable or even better than those achieved for CPWs implemented on GaAs or InP substrates [12], demonstrating the feasibility of mm-wave interconnects on GaN-on-Si epilayer stacks, and by the same token, the viability of a low-cost AlGaN/GaN HEMT MMIC technology on HR-Si. Finally, our work establishes that the high losses of ~3 dB/mm at 2 GHz reported by others [13] for CPWs on GaN-on-Si are simply not representative of a mature GaN-on-Si process technology.

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ACRONYMS

HEMT: High Electron Mobility Transistor
HR-Si: High-Resistivity Silicon
ICP: Inductively-Coupled Plasma
RIE: Reactive Ion Etching
TLM: Transmission Line Measurement