

A New Method for Creating Sloped Resist Profiles Using Mask Structures

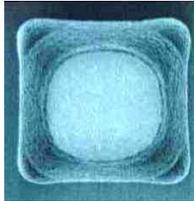
Jens Riege, Samuel Mony, Nercy Ebrahimi

Skyworks Solutions, Inc.
2427 West Hillcrest Drive, Newbury Park, CA 91320
jens.riege@skyworksinc.com (805) 480-4434

Keywords: Sloped Resist Profile, Wall Angle Bossung Curve

Abstract

A common photolithography requirement is to generate a slope in a developed resist pattern prior to etch. To generate the sloped profile the resist is either exposed out of focus, hard baked after develop to flow the resist, or eroded as part of the subsequent etch process. Each of these options requires control of multiple processes to generate a slope that is uniform across the wafer, between wafers and between lots. In this feasibility study, Skyworks evaluated one new approach that uses mask features below the resolution limit of the stepper to expose away part of the resist around the edges of designed features.



INTRODUCTION

Resist patterns viewed directly after develop often have near-vertical sidewall profiles when the process focus and exposure are optimized for critical dimension process control. In photolithography steps prior to metal deposition, however, abrupt topography changes may not be desirable. Evaporated metal structures over sharp topography generally do not deposit in a continuous film, and can form cracks that make a device susceptible to moisture ingress, corrosion or device reliability failure.

It is therefore advantageous to have a gradually sloping resist profile that can be transferred into an underlying material layer during the subsequent etch step. This etched contact via opening then has a gradual slope to assist with an even film during the metal contact formation.

The easiest approach is to “hard bake” the resist, between 120 and 130 deg C for Novolak resin based resists using an oven bake, or a hotplate. At these temperatures the resist softens and begins to flow at the edges of the patterns. Above this temperature range the resist becomes harder to remove, and may start to cure making removal extremely difficult. Oven temperature uniformity can be difficult to

control across the oven, sometimes varying up to $\pm 4^\circ\text{C}$. This variation across a lot of wafers, and across multiple lots loaded together in the oven generates a wide range of slope uniformity. A hotplate bake process provides better uniformity between wafers with temperature control ranging $\pm 0.5^\circ\text{C}$ or better. However, a hard bake process variation to the resist profile is additive to the variation due just to the exposure process.

Another approach to create a sloped profile is to defocus the resist. This method limits the variation to just the exposure process, but large offsets can result in a loss in critical dimension control for the contact via opening. Additionally, focus control at the edge of the wafer can be difficult with some steppers. At the edges of the wafer the laser focus algorithms generally do not have enough data to calculate stepper field planarity and must average focus measurements from partial data or use data from adjacent stepper fields. The variation in focus at the edge of the wafer can generate inconsistent resist sloped profiles, and can generate poor CD uniformity which increases when defocussing a resist to generate a sloped profile.

A third approach is to use a dry etch process to erode the edges of the resist as it etches the underlying film layer. If the etch non-uniformity is radial, this non-uniformity is transferred first into the resist and then into the etched layer under the resist. The variation of this process on the sloped profile is also additive to the variation due to the exposure process and can worsen CD uniformity.

For a 2.5 μm resist photo process over a polyimide film, a 2 μm square via mask feature can result in a round via pattern with a sloped profile at 80 degs when the image is defocused during exposure at -1.5 μm (see Fig 1a,b).



Fig 1a: Via Mask Design
(2.0 μm square)



Fig 1b: Patterned Via

It is possible to get a resist wall angle of 77 deg with a defocus of -3 um, but this defocus makes it difficult to control the via opening dimensions at the bottom of the via. (See Fig 2) .

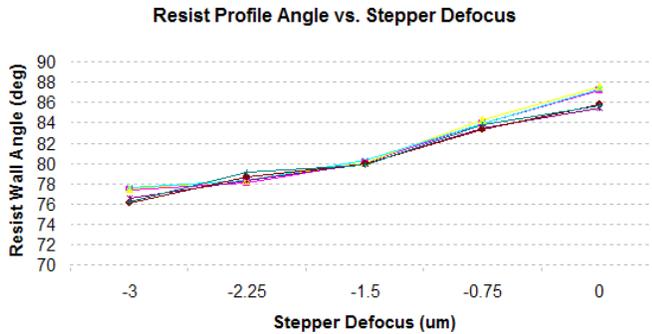


Fig 2: Resist Profile Angle at two wafer locations on three wafers.

THE FIRST ITERATION

One way to address the tradeoff between resist profile and CD control is to generate a sloped resist profile by adding features to an existing mask design. A test reticle was made with three different mask structure designs added around a test via opening: Concentric Rings, Radial Lines and a Grid Array (See Figure 3). Each of these designs were placed around seven square via sizes (0.6, 0.9, 1.2, 1.5, 2.1, 3.0 and 3.6 microns). Each of these replications was designed using two grid sizes (0.1 and 0.15 um squares) for a total of 42 different test structures. On all designs, the corners were weighted more heavily with serifs to maintain the square shape of the via after wafer develop.

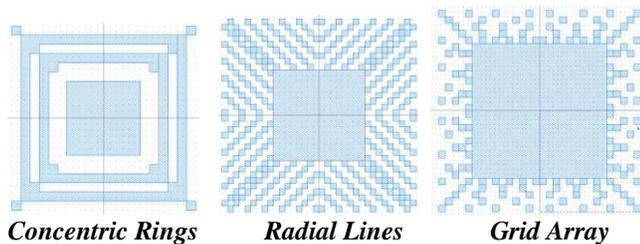


Fig 3: Mask Designs, First Iteration
(Mask Polarity Key: Blue = Clear, White = Chrome)

Results from all of these variations showed only the concentric ring patterns with a resolution of 0.15 um generated a significant sloped wall profile, when used on an i-line stepper with a lens resolution of 0.5 um. (See figures 4, 5, 6)

While showing little impact on resist slope with the 0.10 um mask grid, at 0.15 um mask grid the concentric ring mask demonstrated that the mask features could provide a sloped profile. It also revealed an asymmetry on one of our steppers

due to a lens aberration, known as coma. This asymmetry was not present when this mask was exposed on another stepper.

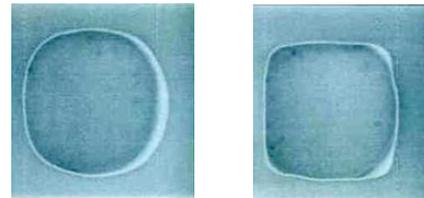


Fig 4a, b: Radial Line Structures using 0.10 and 0.15 um mask grid size

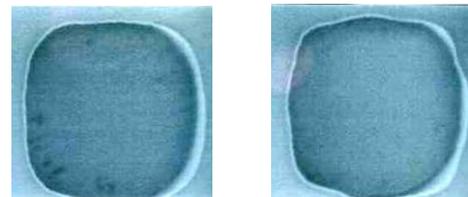


Fig 5a, b: Grid Array Structures using 0.10 and 0.15 mask grid size

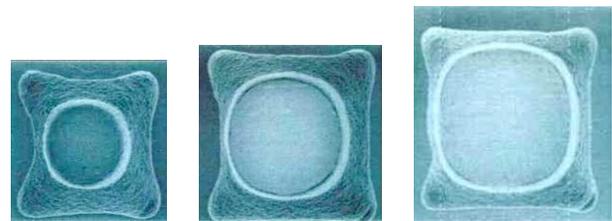


Fig 6a,b,c: Concentric Ring Structures with 0.9, 1.5, 2.1 um Square vias using 0.15 um mask grid

THE SECOND ITERATION

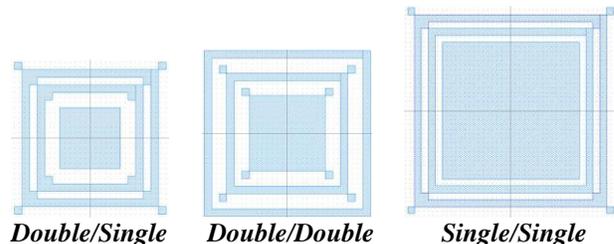


Fig 7: Mask Designs, Second Iteration:
Concentric Ring Spacing

With the design choices narrowed to the concentric ring pattern on a 0.15 mask grid, a second mask iteration evaluated the spacing and pitch of the concentric rings around each via (See Fig 7).

To minimize the number of structures required, the double / single design was placed around 0.6 and 1.2 um square vias, the double /double design around 0.9, 1.5, and 2.1 um vias and the single / single design around 3.0 and, 3.6 um vias. "Double" refers to a 0.30 um wide chrome ring surrounded

by a 0.15 um wide ring opening, and “Single” refers to a 0.15 um chrome ring with a 0.15 um wide ring opening.

For this experiment g-line and i-line resists were used at two focus settings, 0 and -3. In all design iterations, the lowest wall angle was achieved with the double / double concentric ring designs. This corresponds to the mask structures with the 0.9, 1.5 and 2.1um via sizes. The 0.6 um via with the double /single design did not resolve for all focus settings so it was, the design was not practical for this small via size (see Fig 8).

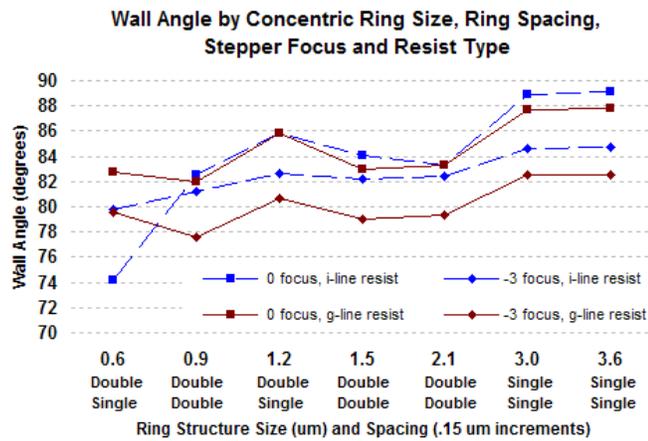


Fig 8: Wall Angle results for various concentric ring spacings, via sizes and resist types at two focus settings.

The 3.0 and 3.6 um vias with the single / single ring spacing show very little variation with exposure energy but generate a wall angle not much better than the control group. Therefore these structures were not considered further.

A NEW METRIC: WALL ANGLE BOSSUNG CURVES

To optimize a stepper process, typically a focus-expose matrix is used to plot critical line width data. The resulting graph, or Bossung curve, plots the line width as a function of focus and exposure. The optimum process window is defined as the region where a curve is the flattest (changes the least) over the largest focus range and exposure range.

In Figure 9, a different type of Bossung curve is plotted for the two via designs and a control group with no design enhancements. These curves are Wall Angle Bossung Curves in that they combine both the top and bottom resist measurements into the resist wall angle calculation, using an assumption of a linear slope. This data was collected using two wafers sequentially coated with i-line resist, exposed sequentially with overlapping focus-expose matrices on the same stepper, and developed together on the same develop track. The gap between the data at -1.5 um focus suggests that wafer-to-wafer variation and edge field focus variation

may be responsible for a 1 to 2 degree wall angle shift between wafers.

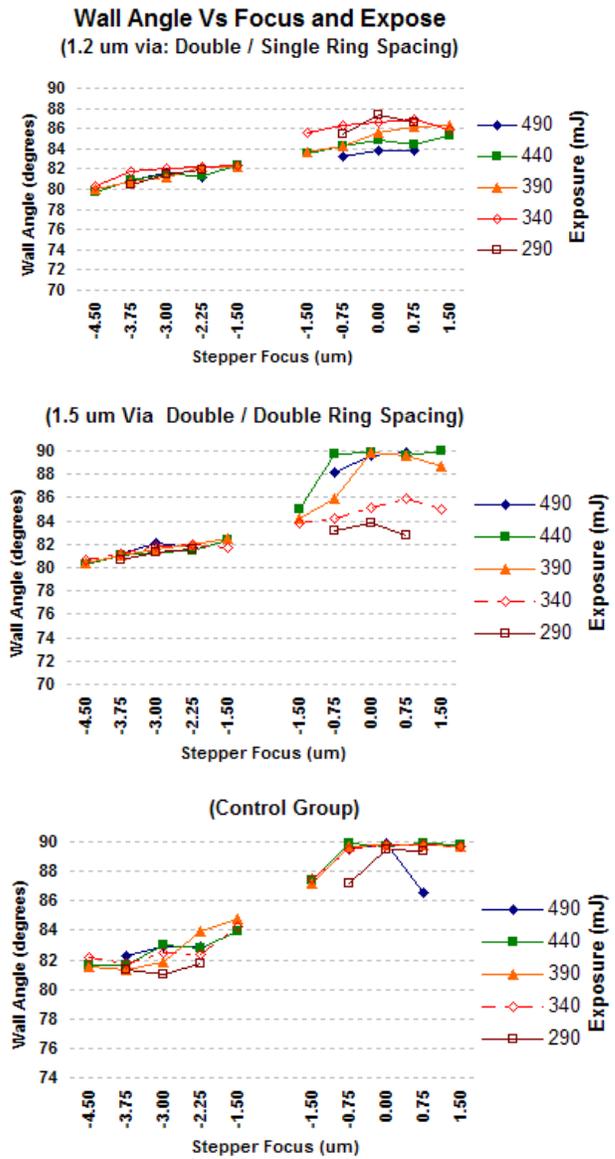


Fig 9a,b,c : Wall Angle Bossung Curves for Double /Single concentric ring designs, Double / Double ring designs, and Control Group with no mask features added

In all Wall Angle Bossung Curves the flattest region and optimum depth of focus for wall angle control was in the vicinity of -3 um focus. Some sites exposed at +1.5 um focus could not be measured due to incompletely opened vias.

These Bossung curves show that for the control group with no mask enhancements, the variation in wall angle increases for lower focus settings during exposure. However, using these mask designs, make it possible to reduce this variation of wall angle to achieve a sloped profile at a lower focus.

The 1.2 μm via with the double / single design shows the best of both conditions: a sloped wall profile with a good depth of focus across multiple exposure settings, and a relatively linear (predictable) change in wall angle with increasing focus for various exposure settings.

A TURN-ON EXPOSURE THRESHOLD

One factor still to be evaluated was the effect of develop time on these structures. It immediately became apparent that these structures have a “turn-on” exposure energy. The exposure energy must be above a critical threshold energy before sufficient light can expose the ring structures (see Fig 10). The single / single design structures exhibited no turn-on energy, indicating a single / single concentric ring design does not transmit sufficient light to generate the sloped profile.

The double /single design has a lower turn-on energy which suggests the user has a larger process window in which to simultaneously target the critical dimension of the bottom of the via opening as well as the wall angle.

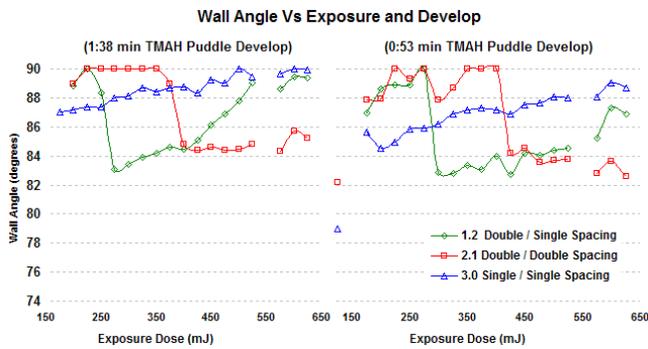


Fig 10: Impact of Develop and Exposure on Via Wall Angle

The difference in the change in wall angle with develop time indicates that the wall angle process window is larger with shorter develop times as long as the develop time is long enough to fully open the via.

FURTHER WORK

This work has not addressed the impact of other process variables such as different resist thicknesses, softbake parameters, or if desired, enhancing the effect of these designs with an added hard bake, or an etch process. These variables should be considered fully when using these structures to characterize the entire process window.

Additionally, it may be possible to further reduce wall angles by adding additional concentric rings. In this case via placement would need sufficient separation to minimize overlap of concentric rings between adjacent vias.

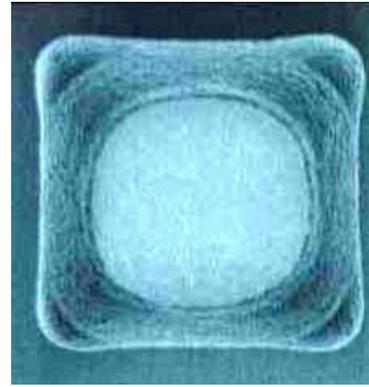


Fig 11: The 1.2 μm Via using the Double/Single Concentric Ring Design

CONCLUSION

A new approach to generating resist profiles has been developed which relies solely on the exposure process. New concentric ring patterns around existing mask structures with a 0.30 μm chrome ring, a 0.15 μm clear ring, a 0.15 μm chrome ring and another 0.15 μm clear ring can generate a sloped wall angle of 80 degrees without the need for flowing the resist(see Fig 11). Serifs added at the corners of the rings help ensure that the corners of a rectangular via shape are preserved. This design has a turn-on exposure threshold in which the wall angle enhancement does not appear until the minimum exposure dose is reached. The concentric ring design is that can generate a sloped resist profile at zero and positive focus settings during wafer exposure. Process controls using develop time, focus and exposure can be used to tailor the process window for the optimum wall angle and critical dimension.

ACKNOWLEDGEMENTS

The authors would like to thank Steve Hovey, currently at Luxtera Inc., for discussions on other mask structures that prompted the inspiration for these designs.

REFERENCES

- [1] Jiro Yota, et. al., *Photodefinable Polybenzoxazole Interlevel Dielectric for GaAs HBT Applications*, 2008 GaAs MANTECH Technical Digest, April 2008.