Characterization of BCB Planarization of Isolated and Dense Features in a High-Topography HBT Process

Tom Dungan

Avago Technologies, Fort Collins, Colorado, thomas.dungan@avagotech.com, 970 288-0026

Keywords: planarization, BCB, design for manufacturability

Abstract

BCB planarization effects across dense and isolated features are characterized both physically through optical measurements and electrically using a maskset designed for that purpose. Yield issues from planarization effects are discussed, along with layout rule methods to guide design for manufacturability in high-topography spin-on-planarized processes.

INTRODUCTION

Spin-on organic dielectrics are useful as planarizing layers in compound semiconductor processes, particularly in processes with relatively high topography and multiple levels of interconnect metal. Such spin-on materials coat over surfaces composed of features of varying heights, partially smoothing the height variations to produce a flattened surface more suitable for fine-feature lithography on following interconnect. However, the planarization is not perfect, so that the top of the dielectric after spin is taller over regions of relatively higher feature density. Two issues caused by such iso-dense planarization effects are variations in depths of vias through the spin-on layer and insufficient dielectric coverage over isolated features.

This paper describes characterization of iso-dense planarization effects through optical depth profiling and through electrical test of structures from a mask set designed to demonstrate the extremes of the dielectric thickness range in an RF HBT process. Methods are also described to predict layout-dependent thickness variation from density computations of various feature layers, weighted by feature thickness, with the resulting weighted-density computation implemented in a design rule checker to give feedback to designers on improving manufacturability of product designs.

PROCESS DESRIPTION

This work was performed as part of development of a process for manufacturing GaAs HBT radio frequency power amplifiers. To meet ruggedness specifications under mismatched load conditions, power amplifier output stages must be constructed of transistors with high collector-base breakdown voltage. This need for high breakdown voltage often forces used of relatively thick collector epitaxial layers. Conventional mesa isolation of such thick collector layers then results in relatively thick (typically > 1μm) steps in the etched semiconductor surface. In addition, efficient layout of dense high-power transistors requires use of relatively thick metallization layers, for low-loss electrical connection, and in some cases for thermal management. For the example HBT power amplifier process used here to demonstrate spin-on interlayer dielectric characterization issues, the relevant topography is pictorially illustrated in Figure 1. The figure schematically shows a mesa of two micron height, with a one-micron-thick metal layer both on the level of the subcollector and on top of the mesa. For simplicity, the details of the other thinner layers are omitted from the figure (e.g., emitter mesa and metallization on top of base mesa, or thin film resistors on the subcollector level).

The planarizing spin-on interlayer dielectric layer is applied over the mesa and lower metal features, with vias through the dielectric formed by subsequent etching and plating. Thus the dielectric needs to be thick enough to submerge the tallest features (preventing shorting to an overlying plated metal layer) while also being thin enough to accommodate the characterized process capability of the via formation process.

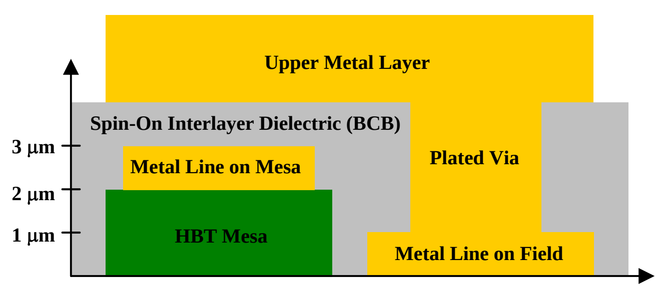

Figure 1. Schematic depiction of power HBT process, showing a HBT mesa of two micron height a one-micron-high metal line over field and over the mesa. (Note that the two micron mesa height includes the effective height of other on-mesa features such as emitter mesa or emitter or base contact metals.)

The evaluation results reported in this paper specifically concern planarization performance of non-photosensitive BenzoCycloButene (BCB) as developed by Dow Chemical Company, however the concerns and the methodology are applicable to other semi-planarizing spin-on dielectrics, such as polyimides.

DENSITY-INDUCED PLANARIZATION EFFECTS

Spin-on dielectrics provide very good local planarization (on a horizontal scale of a few microns) over steps which are smaller than the depth of the dielectric as spun on a flat wafer [1]. However, over larger horizontal scales (perhaps hundreds of microns) the planarization is incomplete. Consider, for example, a three micron thick (flat wafer) BCB film spun over a wafer with only a semi-infinite field region and a semi-infinite two-micron-high mesa. Over the field far from the mesa, the top of the BCB will lie three microns above the substrate, and over mesa near the step up from field the BCB will initially be close to one micron thick. However, in the middle of the mesa far from the field, the BCB thickness over the mesa will eventually build up its full three micron flat-wafer value, so that the mesa plus BCB will be five microns high as referenced from the substrate. In other words, the possible planarized height range going from absolute isolation (infinite field) to absolute density (infinite feature) is simply the total flat-wafer thickness of the deposited BCB film.

Rigorously designing a process to handle this entire theoretical height range could be quite difficult. Consider, for example, a process with features like those shown in Figure 1, using a flat-wafer BCB thickness of four microns (sufficient to cover the tallest features when isolated, with a micron of margin) and a three-micron drawn via dimension. In a region of minimum density, the BCB thickness over field would be four microns, and the depth of a via to an isolated metal line over field would be three microns, for a manageable via aspect ratio of 1:1 (depth/width). However, in a region near maximum density, the via depth could increase to six microns (three microns maximum feature height plus four microns full-thickness BCB minus one micron bottom metal thickness), for a much more difficult 2:1 aspect ratio via.

Planarization length for BCB is relatively long – a feature would need to be several hundred microns across for the BCB to attain full thickness – so in practical RF integrated circuits, the observed planarized height variation will always be less than the flat wafer depth of the BCB. For example, Figure 2 shows a planarized height profile measured optically for a process-development reticle set including a variety of integrated RF circuits. The feature heights for the process used in this example are roughly those of Figure 1, with roughly a three micron flat-wafer BCB thickness. The measured thickness at any point results from the integrated effects of the density of features in over a wide surrounding region. The maximum planarized height range across the representative power-amplifier designs is typically about one micron, considerably less than the three micron maximum theoretical range.

ELECTRICAL CHARACTERIZATION

In order to quantify the ranges of density-induced BCB thickness variation which might occur in various designs, a set of electrical test structures have been designed. The test structures are of two basic sorts, designed to test for the two fundamental failure modes associated with density effects in spin-on dielectrics: open vias in dense regions (thick BCB) and shorting of overlying metal to unrelated tall features in isolated regions (thin BCB).

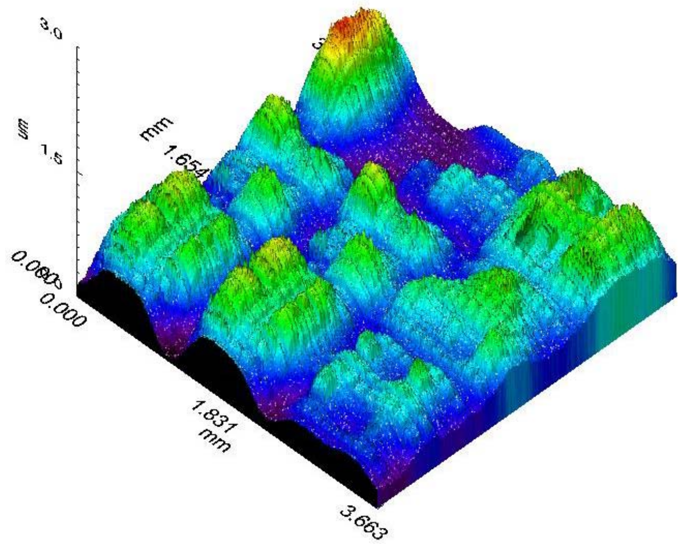

Figure 2. Three-dimensional representation of optically measured surface height profile after BCB planarization of a field from a process development reticle set including many different RF integrated circuit designs.

The test structure for open vias in dense areas consists of a via chain with links in upper-level metal and in lower metal over field, meandering between features of different heights (metal, mesa, or mesa plus metal) of varying dimensions. The structure to test for shorts consists of a lower metal line terminating on a minimum mesa crossed by an overlying upper metal line. This minimum mesa is surrounded by an annulus of lower metal, or of mesa, or of mesa covered by metal at different distances to create different effective densities. The width of the via-chain open-sensor structures was kept at 1000 microns, with heights of 50, 100, 1000, and 2000 microns. The annulus surrounding the short-sensors was similarly varied from 200 to 2000 microns.

Figure 3 shows a view of the entire 2cm x 2cm reticle field for the density characterization test mask, alongside an optical height map of a fabricated set of structures covered with BCB. In the optical image, brighter regions are taller. In the extreme upper left of the optical image, there is a dark 2x2mm region and a bright 2x2mm region – the dark region is essentially empty field, and the bright square is essentially solid mesa plus metal. The measured height difference between the center of these two squares is 3.1 microns, corresponding to the full flat-wafer thickness of the applied BCB. The other structures step methodically through different the different effective densities which could be generated by the designs in the process, allowing electrical confirmation of the process capability to reliably form vias while preventing unintended inter-layer shorts.

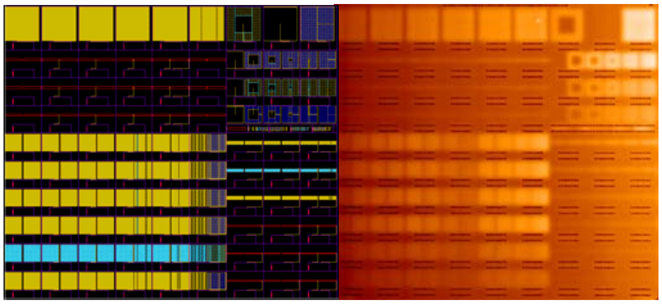

Figure 3. Density characterization reticle field layout shown side-by-side with corresponding measured optical height map after BCB deposition. Brighter regions in image at right indicate taller features after inter-level-dielectric deposition.

An example of electrical measurements from the density characterization maskset is shown in Figure 4. The figure plots the yield of the via chains meandering through 1000 micron x 1000 micron regions of density features consisting of base mesa covered by metal. Each "Duty Cycle" on the horizontal axis of the figure represents a different test structure with the indicated ratio of empty field to density feature. Note that the length of the metal links in the via chains are adjusted in each structure to maintain an equal number of vias. The vertical axis is the yield measured for each particular test structure on a experimental wafer lot. The two different curves are the results from two different process splits varying the flat-wafer BCB thickness. As can be seen from the figure, the results from the thinner BCB spin show no significant yield loss across the entire density range, while the thicker spin results in linearly decreasing yield beginning at a duty cycle of around 0.7 (i.e., repeating structure of 70% mesa plus metal and 30% field).

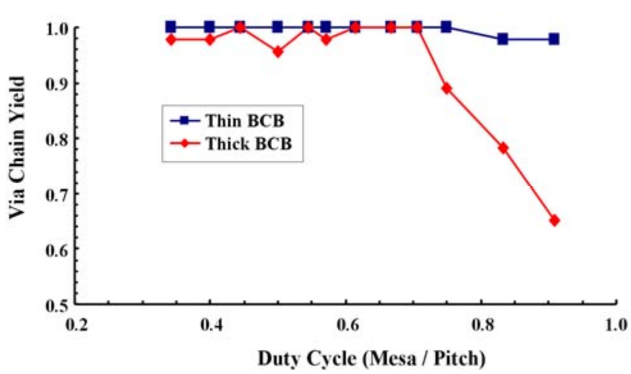

Figure 4. Electrical test results from density characterization mask showing decreasing via chain yield versus increasing density for a thick BCB split, with no significant yield loss for a split with thinner BCB. The drawn via dimension for the test structures shown is 2.6 microns, and the structure area is 1mm x 1mm, with density features composed of base mesas covered by metal.

Figure 5 shows a set of scanning electron microscope images taken from cross sections of test structures representing both extremes of the density range. The two images on the top of the figure are from a wafer with a thinner BCB spin, while the two images at the bottom are from a wafer with thicker BCB spin. The images on the left are from open sensor via-chains of high duty cycle, using mesa with metal as the density feature. The images on the right are from isolated short sensors, with nothing in the vicinity of the isolated mesa for hundreds of microns. As can be seen by examining the figure, the thin BCB spin results in a well-formed deep via in the via chain (top right), but creates a short between upper metal and the metal over the isolated mesa (top left). The images from the wafer with thicker BCB spin show that the isolated feature is not shorted (bottom right), but the deep via is malformed (keyhole plating void is produced by the increasingly retrograde sidewall angle of the deep via etch, and the bottom nitride is not fully cleared from the center of the via).

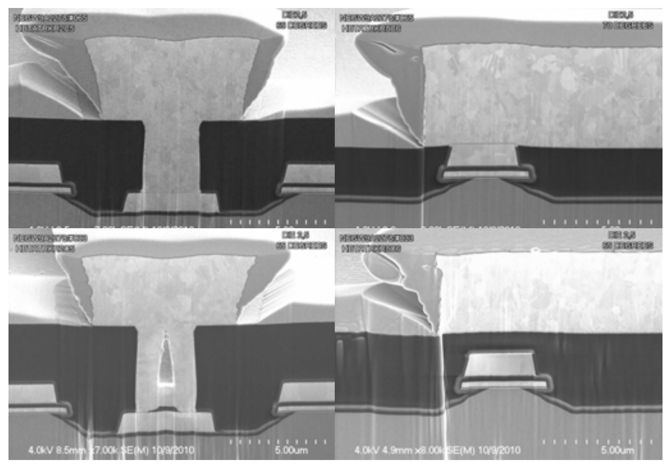

Figure 5. Electron microscope cross-section images from via-chain open-sensors (left) and vertical short sensors (right) taken from a wafer with thin BCB spin (top) and a wafer with thicker BCB spin (bottom). These structures represent density extremes, from very dense in the left images, to very isolated on the right. The thin BCB spin does not provide enough margin to prevent vertical shorting of isolated features (top right), while the thick BCB spin overextends the via process, resulting in keyhole plating void formation and incomplete bottom nitride etch (lower left).

Note that the images shown in Figure 5 are from a short-loop flow using GaAs mechanical substrates with timed wet mesa etch, rather than full epitaxial wafers, resulting in the unusual under-cut mesa shapes visible in the figures. Also note that the incomplete nitride etch at the bottom of the overextended via in the bottom left image helps explain the yield data for such via chains shown in Figure 4, where the yield does not rapidly shift from 100% to 0, but decreases linearly with increasing density for thin BCB. Some fraction of vias begin to be malformed as density increases, prior to the creation of complete opens.

DESIGN FOR MANUFACTURABILITY

Rigorously allowing for full range of theoretical densities (from empty fields to solid metal covered mesas) would require overdesigning the process in ways that compromise other primary deliverables (for example, by increasing minimum via dimensions). Because practical RF designs produce tend to generate only a fraction of the total possible density range, overall optimization is improved if the process is designed for full yield and reliability within only a targeted density window. However, such a strategy requires means to ensure that "pathological" designs outside the intended range will not be released to production. For this purpose, we have implemented numerical assessment of density limits as part of standard design rule checking. Density assessment is somewhat more complex than typical layout rule evaluation, because effective density depends on features on multiple drawing layers, but modern design rule checking tools can efficiently perform such computations.

For our HBT power amplifier process, a weighted density map is computed by averaging the density of features on first metal and base mesa, ignoring features on layers with less significant height. A simple weighting scheme is used, weighting first metal at 0.33, base mesa without overlying first metal at 0.66, and base mesa with overlying first metal at 1.0, according to the respective feature heights. The design is divided into 20x20μm squares, and the spatial weighted-density average is computed for the 400x400μm region surrounding each square. The 400x400μm size for the averaging region was determined by comparing such weighted density computed profiles with optical planarized surface height measurements for representative RF integrated circuit patterns.

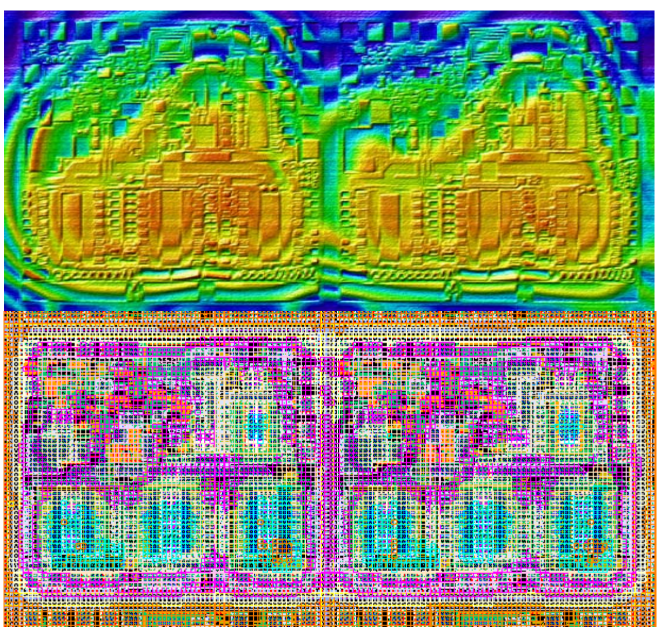

Figure 6. Comparison of optically-measured planarized surface height with design-rule-checker weighted density computation.

Trial application to representative designs indicated that simply flagging all regions outside the density range targeted for the process was too restrictive to design. Instead, violations are highlighted and enforced only when a combination of conditions occurs which could limit yield by creating open vias or by shorting upper metal lines to isolated features. The design rule checker is configured to flag any of the 20x20 micron reporting squares which has a computed weighted density below a certain limit (presently 15% for our process) and also has unrelated upper metal crossing first metal over base mesa, as a shorting risk. Similarly, 20x20 micron reporting squares with a density above a certain value are flagged only if a via through BCB is also present within the 20x20 micron square. Because it is much simpler to correct regions of low density (by the addition of dummy elements around isolated features) than to reduce excessive density, the process is targeted toward tolerance of high density features, with the corresponding limits set such that incidence of open-via risk violations is very rare.

CONCLUSIONS

Performance objectives for mesa-isolated RF power amplifier processes tend to dictate a relatively large topography range, significantly effecting feature formation in isolated verses dense regions of product layouts when using partially-planarizing spin-on dielectrics such as BCB. Methods have been discussed for characterizing such planarization effects physically and electrically, and for enforcing limits to keep designs within the constructed process capability range. By employing such a methodology during process integration, products using planarizing spin-on dielectrics can be optimized for cost, yield, manufacturability, and reliability without sacrificing performance.

ACKNOLEDGEMENTS

Thanks to Andy Weilert for coding of the weighted-density design rule checker in Cadence, to Richard Tuttle for generation of electrical test code, and to the rest of the Avago HBT process development team for discussion, creation of masks, and processing of wafers, and physical analysis.

REFERENCES

[1] T. Stokich, C. Fulks, M. Bernius, D Burdeaux, P. Garrou, and R.H. Heistand, *Planarization with Cyclotene™ 3022 (BCB) Polymer Coatings*, MRS Symposium Proceedings, Vol. 308, 1993

ACRONYMS

HBT: Heterojunction Bipolar Transistor
BCB: Benzocyclobutene