Advances in SiC Substrates for Power and Energy Applications

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Abstract

The progress in the development of 4H-SiC substrates useful for power electronics applications is reviewed. Currently, SiC substrates of diameter 76-100 mm are now commercially available with micropipe defect density <0.1/cm^2 and screw dislocation densities <2000/cm^2. Epitaxial film substrates are manufactured with film thickness up to 25 um, and in R&D with film thickness to 100 um. 4H SiC epiwafers exhibit low values of basal plane defect density. Thick film epiwafers show carrier lifetimes on the order of microseconds. Examples of the use epitaxial substrates in the fabrication of power semiconductor devices provided.

INTRODUCTION

Global focus on electronics technology to control power and reduce energy consumption now drives growth of product markets leveraging semiconductor SiC substrates. Sustained growth requires the availability of SiC epitaxial substrates with continually improving quality and a cost reduction roadmap to support broad product adoption by the power semiconductor industry.

Since 2006, Dow Corning has executed several internal projects and government sponsored programs to develop manufacturing capability to produce 76-100 mm diameter 4H-SiC epiwafer products. Dow Corning has partnered in these programs with end users to qualify the SiC products for power semiconductor device applications. Over this period Dow Corning has leveraged its vertical materials integration capability to create a commercial SiC substrate supply chain based on the application of unique chemistries and materials integration strategies. Inherent to this effort are focus on specific product metric improvements to address the key materials issues limiting the full performance advantages of SiC devices. Priorities included micropipes, epitaxy defects, carrier lifetime, crystal dislocations and thick epitaxy.

Reduction of Dislocations in 4H SiC Crystals and Wafers

In 2006, experimental work began to focus on heavily doped (n+) 4H-SiC crystal growth and CVD epitaxy processes with the goal to develop an epitaxial wafer product to address anticipated rapid growth in the use of SiC in power electronics.

PVT 4H-SiC crystal growth rapidly achieved the 76 mm wafer generation milestone with micropipe density <10/cm^2. This was accomplished by design of experiments optimization of thermal fields and vapor chemistry, coupled with manufacturing disciplines to insure consistency. The process reached a point of maturity where further reduction of micropipes, dislocations and grain boundaries was limited. In order to achieve the needed step change improvement in crystal quality, several changes were made in the crystal growth arrangement (furnace, reaction cell, process chemistry) with the goal to radically alter the sources of stress in the growing crystal. Figure 1 shows that these alterations achieved the desired results, a repeatable process with the capability to reduce micropipes to <0.1/cm^2 along with a step change reduction in the total screw dislocation density.

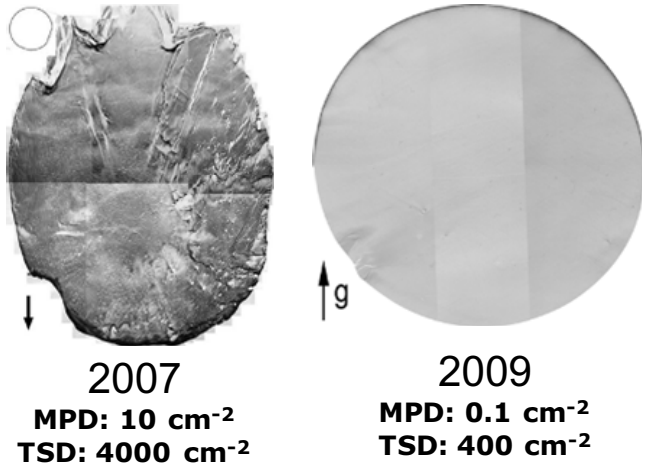

Figure 1. Reflection x-ray topography (XRT) images of 76 mm diameter n+ 4H SiC crystals. Left: Original PVT Process; Right: Improved PVT Process.

Repeated use of the improved PVT configuration revealed that the process could dissolve micropipes unit dislocations and readily relaxed areas of concentrated stress in SiC crystals [1], positively impacting dislocation generation.

Figure 2 shows the chronological reduction in micropipes in conducting 4H SiC wafers achieved through the manufacturing implementation of Dow Corning's PVT process technology. Currently the median micropipe defect level is below 0.1/cm^2.

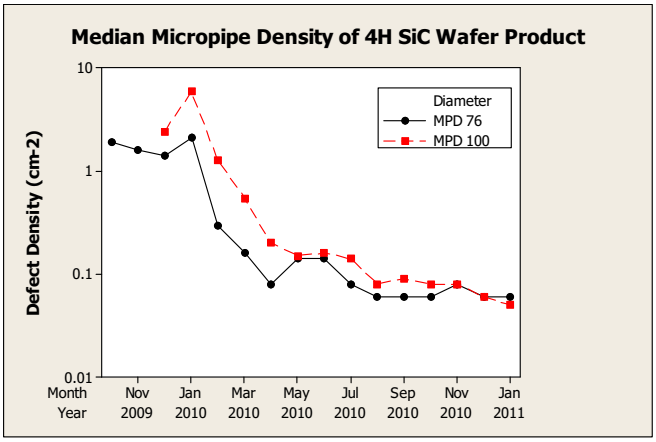

Figure 2. Median micropipe defect density of conducting 4H SiC wafers of both 76 mm and 100 mm diameter manufactured over five quarters.

Detailed measurements of screw dislocations were performed on numerous 76 mm diameter 4H SiC crystals and consistently revealed very low levels of screw dislocations. The statistical distribution of screw dislocations in the family of crystals is shown in Figure 3.

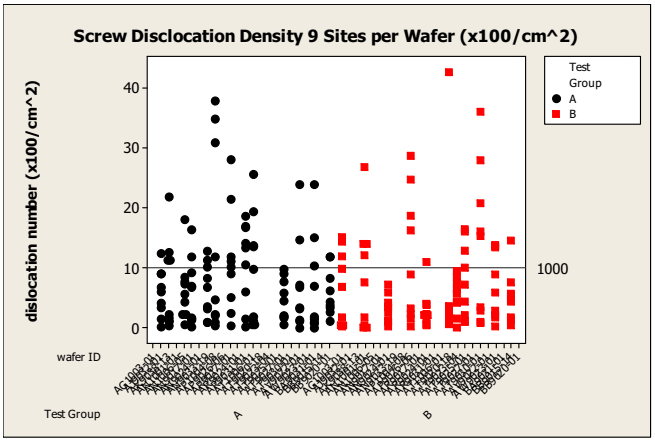

Figure 3. Measurements of screw dislocation density on wafers from over 25 crystals of n+ 4H SiC. Data was collected by x-ray topography and counting was performed at nine sites on each wafer. Each column of points represents the nine measurements on each wafer. The groups represent two sampling points of manufactured product over the period from midyear 2009 to midyear 2010.

Continued improvements in SiC crystal growth successfully produced families of seed crystals with this low dislocation density and no detectable micropipes. These crystals are now leveraged in manufacturing 4H SiC crystals for both 76 mm and 100 mm diameter wafers. X-ray topography analyses of 4H SiC crystals also revealed that the stress control improvements in the PVT process technology was capable of producing crystals with very low basal plane defect (BPD) density, achieving almost 3 orders of magnitude reduction compared to values typically reported in the literature [2,3]. 4H SiC wafers manufactured today at Dow Corning typically show BPD density ranging 0-1000/cm2 based on multiple site within wafer testing by XRT or molten salt etching.

4H-SiC Epitaxy Substrates for Power Electronics Applications.

To meet the materials performance standards in power electronic semiconductor device fabrication, very low defect wafers must be processed with low defect epitaxial layers. Uniformity of doping and thickness is critical to all power diode and transistor processing. Most of the power devices made today with SiC are junction barrier Schottky diodes, JFETs and MOSFETs. The benefits of SiC are particularly advantageous in fabrication of bipolar devices such as PiN diodes and thyristors, especially when they can be fabricated with epitaxial layers up to and beyond 100 um thickness.

Dow Corning has developed research and manufacturing CVD epitaxy process technology for 4H SiC epitaxial layers of up to 100 um thickness on substrates tilted 4 deg. toward <11-20>. The most important metric in epitaxial wafers is defects added during the epitaxy process. With the extremely low MPD levels in today's 4H-SiC wafers, epitaxy related defects are likely the largest material related source of yield loss in device fabrication. The impact of epitaxy defects is best assessed by laser light scattering spectrometry. The wafer is divided into area sites and each site is inspected using a laser light scanning spectrometer [4]. Sites containing defects are marked as failures and the defect density determined using a Poisson distribution model. Figure 4 shows the performance of total defect density (wafer and epitaxy combined) for Dow Corning's 76 mm diameter substrate epitaxy manufacturing as determined for 5 consecutive quarters.

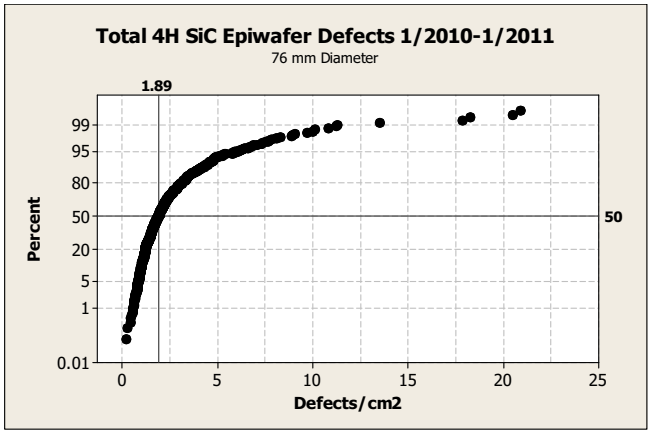

Figure 4. Distribution of total defects (substrate and epitaxy added defect, inclusive) for 76 mm diameter production 4H SiC epiwafers measured by laser light scattering spectrometry. Thickness of the epitaxial films typically in the range of 5-15 um.

The laser light scattering data shows that median total defect density over this period is approximately 1.9/cm^2. Put in terms of potential impact on within wafer device yield, this defect density value corresponds to a theoretical device yield

93% for 2x2 mm die sites and 48% for 5x5 mm die sites using a Poisson model.

Optimized CVD epitaxy processes are known to reduce the density of BPDs which propagate into the epitaxial layer [5,6,7]. Starting with low BPD density substrates and an optimized epitaxy process, epiwafers with extremely low BPD levels ranging 0-2/cm^2 have been observed on large areas of 76 mm diameter substrates by UV-PL and also molten salt etching tests [8].

Throughout the government sponsored research programs between 2006-2010, many wafers were supplied for fabrication of Schottky and PiN diodes by industry partners, with the goal to achieve clear correlation between materials defects and blocking voltages. In 2009 results were presented showing near theoretical blocking voltage and forward voltage drops were achieved on 2 kV SiC PiN diodes [9]. Similar performance was routinely achieved on junction barrier Schottky diodes. Figure 5 presents an example the distribution of blocking voltage achieved using 4H-SiC epiwafer with 8.3 um of epitaxy with average doping of 1.6E16/cm^3. Rule of thumb of blocking capability is typically 100 V/um of epitaxy, or in this example, ~850 V. Theoretical blocking voltage based on the wafer resistivity and epilayer metrics is ~1250 V. The figure shows that over 50% of the die on the wafer operate at near theoretical performance for 4H SiC, and over 90% of the die block >1000 V. This example is representative of the operation potential of SiC diodes when both the materials and device fabrication are optimized.

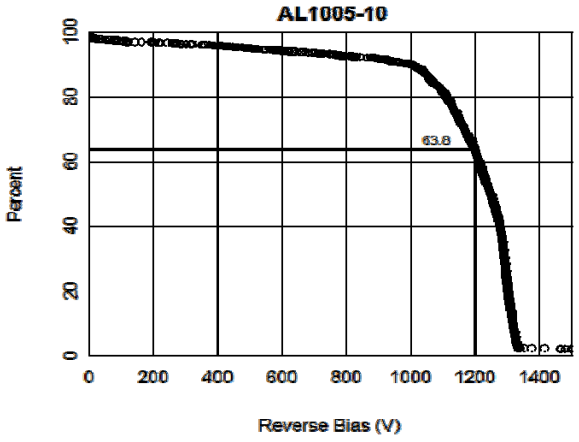

Figure 5. Distribution of diode blocking voltages measured on 76 mm diameter 4H SiC epiwafer, 8.3 um thick, average doping 1.6E16/cm^3.

Reduction of crystalline, epitaxial and electrical defects must happen in concert to accelerate advancements in SiC devices for high voltage (3-15 kV) applications. In late 2009 new research efforts in CVD SiC homoepitaxy the targeted film thickness ranging of 50-150 um. Figure 6 shows an example of the morphology of a optimized 4H SiC, 4 deg. tilt epiwafer with 100 um thick film doped <1E15/cm^3. The surface shows very little defectivity and minimum step bunching.

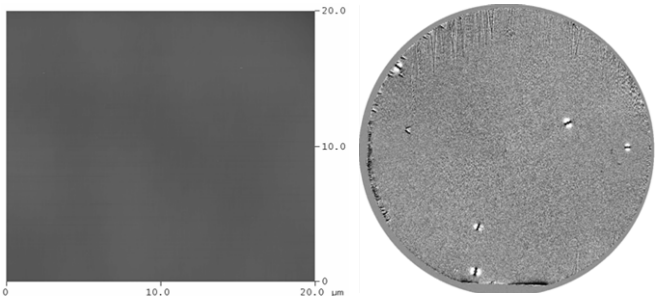

Figure 6. AFM image of the wafer center (left) and whole wafer laser light scattering topograph image (right) of a 76mm diameter 4H SiC wafer with 100 um epitaxy. The AFM image is featureless and shows average roughness is 0.7 nm. The measured total defect density is 1.9/cm^2.

Figure 7 shows the distribution of total epitaxy wafer defect density as a function of epitaxy thickness achieved in the thick epitaxy effort. Compared to production epitaxy (Fig.4), the median defect levels are slightly increased as epitaxy thickness is increased to 80 um, and higher still above 80 um.

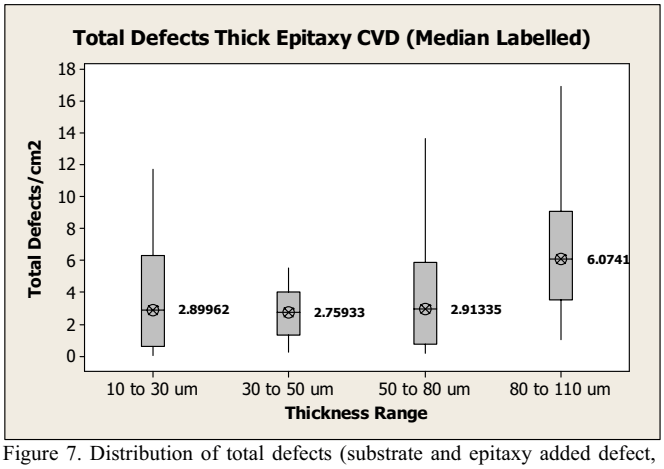

Figure 7. Distribution of total defects (substrate and epitaxy added defect, inclusive) in 76 mm diameter research 4H SiC epiwafers for high voltage applications measured by laser light scattering spectrometry.

Additional optimization of the in thick epitaxy CVD process will stabilize the performance to the level shown in Fig. 6, driving it to parity with the standard production epitaxy performance.

Carrier lifetime is a critical parameter in SiC epitaxy as low lifetime values limit the minimum forward voltage in bipolar devices. Dow Corning has reported state of the art carrier lifetime values in 4H SiC epitaxy and device results confirming longer lifetime values will minimize voltage drop in PiN diodes [10,11,9]. Measured using microwave photoconductive decay, epiwafers of average thickness 80-100 um and doping level approximately 1x10^{14}/cm^3 typically exhibit a range of mean lifetime values between 3-6 µsec at injection levels of about 1E16/cm^3, with best average values approaching 15 µsec and lowest

approximately 1 μsec. The source of the range of lifetime values is not understood, but one possibility is large variations in the surface recombination rates between epitaxy processes. In general, the data reported from microwave photoconductive decay measurements represents a conservative estimate of the bulk carrier lifetime as surface recombination will act to reduce the apparent value of the carrier lifetime.

At the time of writing, first blocking voltage results of junction barrier Schottky diodes fabricated on 50 um thick epiwafers continue the trend observed in 0.5-2.0 kV diodes with respect to very high blocking voltage. Diodes of area ranging 3-50 mm^2 were fabricated on several wafers with doping in the range 6-8E14/cm^3. Figure 8 shows an example of the blocking results as a function of diode size.

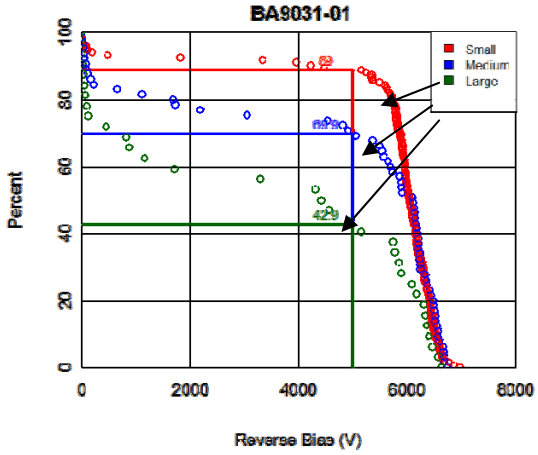

Figure 8. Distribution of diode blocking voltages measured on 76 mm diameter 4H SiC epiwafer, averaging 52 um thick, with average doping 8.5E14/cm^3.

Diodes with blocking voltages exceeding 6 kV were observed on all wafers. A simple estimate characteristic defect density of the process can be obtained using the Poisson equation

$$Y = e^{-A*Do}$$

Where Y is the fractional yield associated with devices of area A. D_o is the characteristic defect density and is obtained from the slope of the log-normal plot of yield versus die area. This equation can be applied using the blocking voltage data and also using data from the defect distribution obtained by laser light scattering tests on the epitaxial wafer, in this case setting a site size and failing sites with a light scatter defect. Using the laser light scattering spectrometry data the characteristic defect density for the 50 um epiwafer set ranges 1.0-1.4/cm^3. Analysis of the die yield at 5 kV or greater blocking vs. die area results in a slightly higher defect density ranging 1.7-2.4/cm^3.

CONCLUSIONS

4H SiC conducting wafers and epitaxy have been successfully developed into products to address the needs of emerging power and energy efficiency applications. Current defect levels below 2.0/cm^2 in epiwafers can produce favorable manufacturing yields for power devices in the 600-2000 V, 5-50A range. Dow Corning has now added research efforts to extend the epitaxy materials performance for high voltage applications for the energy grid. Future work includes development of SiC wafer products with diameters of 150 mm to drive cost reduction of SiC devices to achieve cost parity with silicon power devices.

ACKNOWLEDGEMENTS

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REFERENCES

[1] D.M. Hansen, M.J. Loboda, R.V. Drachev, E.K. Sanchez, J. Zhang, E.P. Carlson, J. Wan, G. Chung, Mater. Res. Soc. Symp. Proc. Vol 1246, 2010, p.21

[2] N. Zhang, Y. Zhang, B. Raghothamachar, S. Byrappa, G. Choi, E.K. Sanchez, D.M. Hansen, M.J. Loboda, Mater. Sci. Forum 645-648, 2010, p.291

[3] M. Dudley, S. Byrappa, F. Wang, Y. Zu, Y. Zhang, B. Raghothamachar, G. Choi, E.K. Sanchez, D.M. Hansen, R. Drachev, M.J. Loboda, Mater. Res. Soc. Symp. Proc. Vol 1246, 2010, p.29

[4] J. Wan, S.-H. Park, G. Chung, and M.J. Loboda, J. Electronic Materials, Vol. 34 (10), p.1342

[5] Z. Zhang, T.S. Sudarshan: Applied Physics Letters 87, 151913 (2005).

[6] W. Chen, M.A. Capano: Journal of Applied Physics 98, 114907 (2005).

[7] T. Ohno et al.: J. Crystal Growth 260, p. 209-216 (2004).

[8] G. Chung, M.J. Loboda, J. Zhang, J.W. Wan, E.P. Carlson, T.J. Toth, R.E. Stahlbush, M. Skowronski, R. Berechman, S. G. Sundaresan and R. Singh; 4H-SiC Epitaxy With Very Smooth Surface and Low Basal Plane Dislocation on 4 degree Off-axis Wafer, *to be published in the proceedings of the 2010 European Conference on SiC and Related Materials.*

[9] G. Chung, M. J. Loboda, Sid Sundaresan and Ranbir Singh, Correlation between carrier recombination lifetime and forward voltage drop in 4H-SiC PiN diodes, *to be published in the proceedings of the 2009 Int'l Conference on SiC and Related Materials.*

[10] G. Chung, M.J. Loboda, M.F. MacMillan, J. Wan, D.M. Hansen," Materials Science Forum **556-557**, 323 (2007)

[11] G. Chung, M.J. Loboda, M.F. MacMillan, and J.W. Wan Mat. Sci. Forum, Vols. 615-617 (2009) p287

ACRONYMS

PVT: Physical Vapor Transport
XRT: X-ray topography
MPD: Micropipe density
TSD: Threading screw dislocation
BPD: Basal plane dislocation
JFET: Junction field effect transistor
MOSFET: Metal oxide semiconductor field effect transistor.