Shuffle Up and Deal: the Use of Wafer Randomization as a Yield and Process Analysis Tool

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Abstract

The use of repeated wafer randomization throughout a process flow can be combined with yield or other observables to help identify problematic tools or process steps. This technique can help identify bad chambers in multichamber tools, tool drift, or process dependences which were not previously understood. Although less effective on small lots, the technique is sometimes capable of revealing trends across a series of lots.

INTRODUCTION

In the past 10 to 20 years, GaAs semiconductor products have increasingly gone from low volume niche markets such as military and aerospace components to high volume commodity markets such as mobile wireless [1]. At the same time, circuit complexity and integration have increased. This has driven the need for increased yield and quality control and means that more sophisticated tools must be used to analyze problems than in the past. The silicon industry has had similar transitions in terms of volume and complexity, and their techniques are now being increasingly used by the GaAs industry.

This paper discusses one particular technique, wafer randomization [2], borrowed from silicon fabrication. This technique had been developed and used for over 20 years in what was then an exclusively silicon Hewlett-Packard (later Agilent) fab in Fort Collins. The GaAs processes now used in Fort Collins had their origins in the low-volume Avantek fab in Santa Clara, California, where wafer randomization was not used. When the process transfer was finished in 2002, wafer randomization was added to the GaAs processes to aid in troubleshooting yield and quality problems.

METHOD OF RANDOMIZATION

At multiple steps in the process, lots are put into a wafer sorter tool which randomly reassigns the wafer order in the cassette. This is conceptually similar to shuffling a deck of cards between hands in a card game. At the same time, the tool reads and records the new wafer order in the cassette.

If the wafers later show variability in an observable with a pattern or correlation to wafer order, this information can be used to help troubleshoot what went wrong. Examples of such observables include yield, electrical parameter value, or a visual signature. In some cases, there may already be suspicions about what part of the process caused the variability in the observable, and it might seem clear what part of the process to investigate for the cause of the variability. However, if randomization is carried out multiple times during the suspect section of the process, the wafer order information can help to further remove ambiguity about where the process has gone wrong.

For single lots, wafer randomization is more effective if the lot size is large because patterns are less likely to occur by chance. This will be discussed in further detail later in this paper. If wafer order data for multiple lots also can be combined to reveal patterns, the dependence on a large lot size can be reduced.

Several examples will be discussed below to show how the wafer randomization can be used for yield analysis purposes. In all cases, these examples are drawn from real problems seen in Avago's various pHEMT process flows.

IDENTIFICATION OF MALFUNCTIONING CHAMBERS IN A MULTI-CHAMBER TOOL

One of the more common cases where wafer randomization is of value is where isolated chambers in a multichambered tool have started to impact an observable. In this case, the observable should produce a periodic pattern with wafer order, and the use of randomization should isolate the problem to a single operation or a range of operations.

A fairly simple case occurred in early 2010. Several wafers in a single lot were scrapped for high plated metal sheet resistance. Although several process steps involving the plated metal could be implicated, suspicion immediately fell on the plating process itself. Roughly a quarter of the wafers failed, and the plating tool is one of the few tools which can process four wafers simultaneously in separate chambers. Figure 1 shows what happens when the wafers are sorted in the order through the plater, as well as other orders around the plating operation. This confirms that every fourth wafer during the plating operation failed and drew attention to a specific chamber. It was found that the plating solution in this chamber was not at the proper level and therefore not making good contact with the wafer.

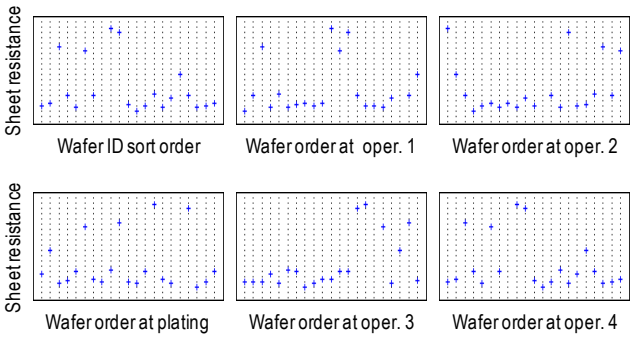

Figure 1. A set of plots showing the median plated metal sheet resistance vs. wafer ID number and wafer order at five operations around and including the plating operation. The plating operation shows a perfect pattern where every fourth wafer has high resistance (note that there is a blank space due to a missing wafer). The other operations show more random dependences.

A more complex case occurred in late 2004 and into early 2005 and involved a major product line. Up to half of the wafers in multiple lots for this product line were being scrapped after failing the product sample test. There were two observables: a particular failure bin for wafer yield, and in some cases, a particular signature on each wafer's bin map consisting of a rough concentric circle with a radius about midway from the wafer center. This pattern had to be subjectively judged by engineering, and examples of this pattern are shown in Figure 2.

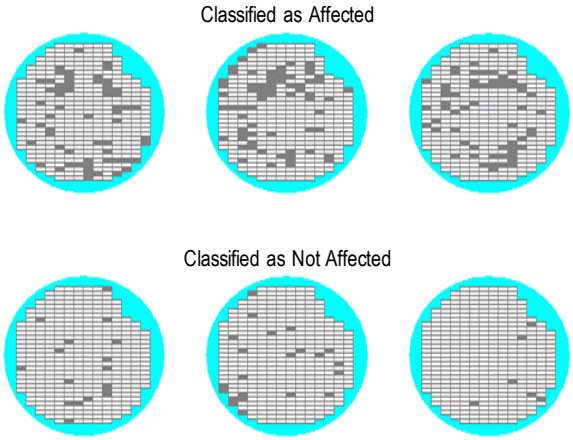

Figure 2. Examples of the sample test bin map signature for affected wafers (top 3 maps) and unaffected wafers (bottom 3 maps). Gray boxes are failing dice; white boxes are passing dice.

Because of the type of yield loss, suspicion focused on the operations involved in gate formation. Gate formation is critical for pHEMT devices and involves a number of operations, including photolithography, etch, and metal formation. Investigation showed that the aforementioned observables were correlated with wafer order within a lot, but only for a small subset of gate formation operations. This wafer order showed an alternating yield pattern, where every other wafer was lower yielding. Wafer orders at other operations didn't correlate with a particular pattern. Furthermore, this pattern could sometimes still be seen, albeit at subtler levels, on lots where most or all wafers passed the product sample test.

Example plots correlating yield or bin map pattern to wafer order for a single lot during this period are shown in Figures 3 and 4. This alternating pattern drew attention to two-chambered tools within this range of operations where wafers alternated between chambers. Experiments later confirmed that one chamber in a two-chambered wet processing tool was responsible for this effect. The bad chamber was temporarily shut down while repairs were made. Differences were found in the nitrogen drying system in each chamber, and matching the two chambers made the yield difference disappear.

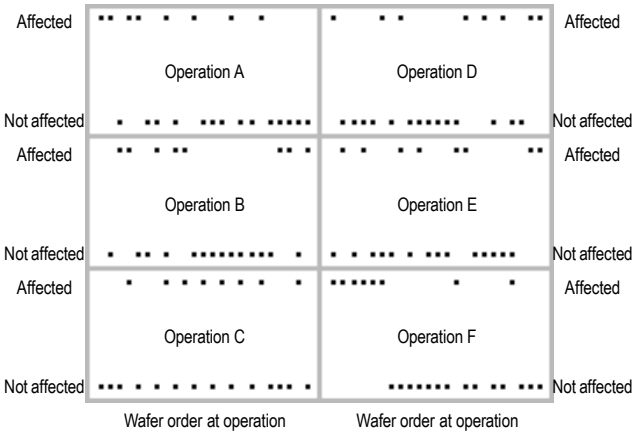

Figure 3. A set of plots showing the presence of the bin map signature vs. wafer order at six different operations on a lot during the late 2004 to early 2005 time frame. Data actually exists for many more operations. Operation C shows a nearly perfect alternating pattern (note that there is a blank space due to a missing wafer). The other operations show much more random dependences.

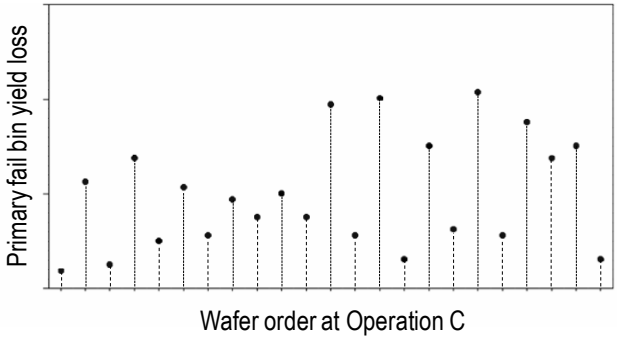

Figure 4. Yield loss from the primary fail bin vs. wafer order at operation C for the same lot as shown in Figure 3. Note that yield loss is in an alternating pattern.

TRENDS WITHIN A SINGLE LOT OR ACROSS LOTS

The techniques can also be used to see trends within single lots, or in some cases, over several lots. A simple example is shown in Figure 5. Here, several wafers failed electrical test on a key parameter. These symptoms looked

quite lethal, but the randomization data quickly traced the problem back to the probe operation itself, rather than an actual processing operation. The probe card was becoming dirty during the test and causing the measurements to be distorted. When the probe card was changed and the lot was retested, the failures disappeared.

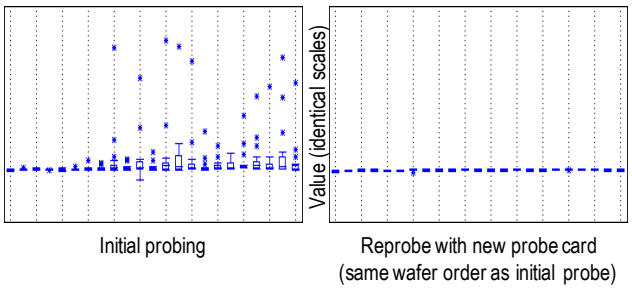

Figure 5. The value of a key electrical parameter vs. wafer order at probing on a single lot, shown as a box plot with points outside the outer fences plotted. The vertical scale is identical between the two plots. The left plot is the initial data; the right plot is reprobe data after the probe card was changed.

In earlier occurrences of this type of probing failure, there was no separate randomization before probing. This could cause a failure to look like it had credibly come from a real process. An improved probe card change schedule was implemented for this prober. A wafer randomization was also added for the probe operation so that these types of problems could be quickly distinguished from true process problems.

Another particular example occurred early in 2006, where a single entire lot was scrapped after all wafers failed for poor PCM transistor breakdown. This particular process family has a strong dependence between some of the gate formation steps and the breakdown. The initial investigation concentrated on the failure of the particular lot, but quickly revealed that other lots in the same process flow had been processed on the same day. These lots didn't fail, and the question was raised as to what had been different about these lots.

As part of the investigation, the breakdown was plotted against the wafer order data for a plasma etch step in this part of the process. This revealed a distinctive pattern which carried over even to lots which passed the same test. The etch tool was being conditioned or burned in during processing, so that the breakdown would increase as more wafers were processed. This pattern, shown in Figure 6, actually spanned all of the lots on that day, and was apparent on other lots processed even a few months earlier. The pattern would only reset itself when a different process was run on the tool. Although this was one of the oldest process families still running at the time, several significant changes were made to this etch process to counter this burn-in effect. In particular, the process originally used a fixed etch time, but was modified to use endpoint detection to make the breakdown more uniform between wafers.

In this particular case, specific steps in the process were immediately suspected based on the historic understanding of the process. Although it can be argued that wafer randomization was less valuable in this case, the use of the wafer randomization data adds considerable certainty by eliminating other steps in the process which could also conceivably have caused the breakdown problem.

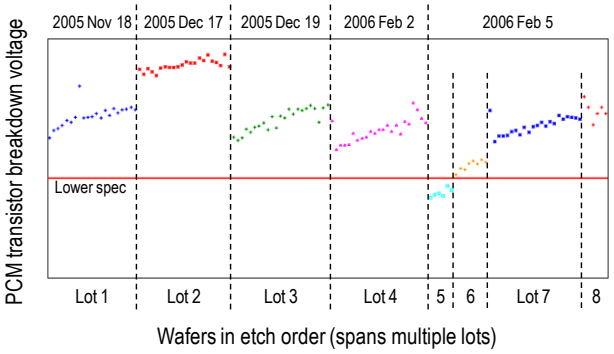

Figure 6. PCM breakdown voltage vs. wafer etch order on multiple lots. Each point shows PCM wafer median. Solid horizontal line indicates spec limit; lot 5 was totally scrapped after failing this limit and triggered this investigation. Note trend of increasing magnitude as more wafers are processed. Four lots were processed consecutively on February 5, 2006, and the trend continues through all 4 lots.

THE POSSIBILITY OF FINDING HIDDEN DEPENDENCES

There is the possibility that the randomization data will show information about a different process than the one which is causing trouble. An indirect and unusual example is presented below.

In the fall of 2005, a new product line was ramping up, and initially the yield was highly variable. One engineer tasked with looking at these yields had found a peculiar dependence: the wafer in slot 5 of the cassette at a particular photolithography step had higher yield for many of these lots. The yield difference was significant, and was at least 10 percentage points higher than the average for the rest of the lot. Inquiries revealed that the wafer in slot 5 was being put into a SEM for routine CD measurement of the resist opening.

The initial reaction to this information was skepticism: why would a metrology tool affect the yield on a wafer so dramatically? However, experiments showed that this effect was real: putting additional wafers in the SEM at this step raised their yields too. For a time, efforts were made to replicate this effect without using the SEM, for instance, by putting the wafers into vacuum chambers or ovens of various types. These other tools were generally not as effective as the SEM in improving the yield, and a satisfactory explanation to how this effect worked was never obtained.

The end solution to the yield problem was to re-examine the photolithography steps in this area of the process. After all the refinements, the yield improved dramatically and the CD-SEM effect was no longer detectable. This solution indirectly suggests an important point about the

randomization pattern seen earlier: the improvements in the photolithography process margin probably only obscure the wafer order pattern at the SEM. To put it another way, it is possible to lose margin on a particular process operation to reveal a hidden pattern in a different process operation. In such cases, correlation to a particular wafer pattern doesn't point to the actual cause of the problem.

WHAT ARE MY ODDS?

It is worth asking whether a pattern is significant in terms of probability: is it likely or unlikely that a given pattern will appear by chance, and therefore, should it be pursued as a cause of a problem? What follows is an analysis of the probability of some very simple patterns. We will assume that there are no missing (broken or scrapped) wafers at the point where the observable can be evaluated. In such cases, the number of ways that the wafers can be ordered can be described by the factorial $n!$ where n is the number of wafers in the lot.

Let's start with a case with alternating wafers. Here we assume that all wafers form a clear bimodal distribution where exactly half are in each group if the number of wafers is even. If the number of wafers is odd, the first group will be assigned as the larger group. It should be noted that the yield in Figure 4 can't strictly be classified this way if the dividing line is drawn at a particular yield. The bin map pattern in Figure 3 can't be strictly classified this way either, but is a more subjective measure.

The wafers can be scrambled within each group and still maintain a perfect alternating pattern over the entire lot. Within the first group, there are then $(n/2)!$ arrangements if n is even, and $[(n+1)/2]!$ arrangements if n is odd. The second group can be treated similarly. Since these two groups are effectively independent, the total number of arrangements with both groups together is $[(n/2)!]^2$ if n is even or $[(n+1)/2]!\cdot[(n-1)/2]!$ if n is odd.

Another case is where the observable can be ranked and the wafers fall perfectly into that rank order. There is then only one ascending rank arrangement and one descending rank arrangement. Figure 6 tends toward this type of behavior, but doesn't fully achieve it. To show a situation which might be more realistic, we can also easily calculate the number of arrangements if one pair is transposed out of order. For example, in a five wafer lot, the perfect rank order is 1,2,3,4,5; but we can have transposed orders **2,1**,3,4,5 or 1,2,**4,3**,5 with the transposed pairs in bold. There are n-1 ways to transpose both the ascending and descending arrangement.

For all of the cases above, the number of arrangements is divided by $n!$ to determine the probability of seeing the pattern. Figure 7 shows the probability of obtaining the aforementioned patterns. The idealized alternating pattern goes below 1% probability with 9 or more wafers. The perfect ranked pattern takes only 5 wafers to go below 1%. The probabilities in Figure 7 are for each randomization. The probability of ever seeing a given pattern appear throughout a lot's entire history by chance will increase as wafers are randomized at more steps in the process. If a lot contains a large number of wafers, this probability will still be very low.

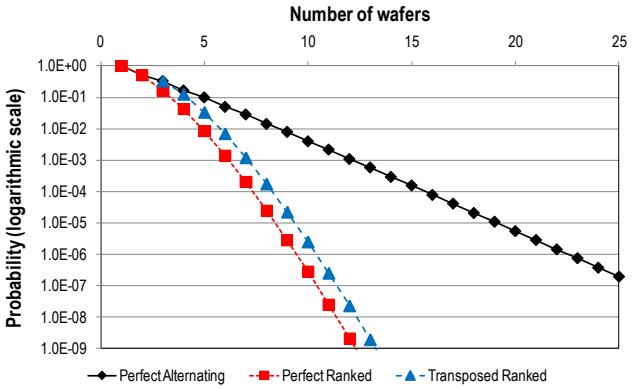

Figure 7. Probability of achieving a perfect alternating pattern, a perfect ranked pattern (either ascending or descending), or a ranked pattern (either ascending or descending) with one adjacent pair transposed; vs. number of wafers.

CONCLUSION

Repeated wafer randomization through the process can be used as an effective tool to aid yield analysis. The use of randomization helps to indicate process dependences which depend on wafer order, while also removing ambiguity about which process step is involved. While more effective on larger lots, the technique can still have value on smaller lots, especially when multiple lots with the same failure patterns are involved. There can also be cases where hidden patterns in one process can be revealed by loss of margin in another process which interacts with it. In such cases, the pattern does not point directly to the cause of the process problem.

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ACRONYMS

CD: critical dimension
PCM: process control monitor
pHEMT: pseudomorphic high electron mobility transistor
SEM: scanning electron microscope