Reducing Broken Thinned GaAs Wafers During Backside Processing

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Keywords: GaAs, Wafers, Broken, Thin

Abstract

Because of the crystallographic structure of GaAs, broken wafers are a fact of life in GaAs fabs. Whether these broken wafers are scrapped or shipped, they represent lost revenue to the company and a headache to assembly houses that have to deal with partial wafers.

A cross functional team was assembled at RFMD to investigate, and implement solutions to reduce the number of broken wafers after all backside processing had been completed. A number of factors across all backside operations were found to contribute to wafer breakage. Some factors were fairly obvious such as final wafer thickness, the rest required more effort to uncover and solve. Important factors include the final glassivation dielectric thickness, bonding medium composition and thickness, makeup of the post-thin stress relief etch solution, gold plating fixture design, and others. We also found significant interaction among some factors.

As a result of these efforts, we were successful in steadily reducing the number of broken wafers to a more acceptable level. Efforts must continue to maintain the present gains, and find additional solutions to continue the downward trend.

INTRODUCTION

The majority of products shipped from RFMD require a final wafer thickness of 100 microns, complete with gold plated backside vias. Thin GaAs wafers are extremely fragile and can not be handled through the various backside processes without adequate mechanical support. This support is usually accomplished by temporarily mounting the wafers on perforated sapphires; once backside processing is complete; the wafers are demounted from the sapphires and are now ready for singulation. Laser dicing is the current method for die singulation and is the final step prior to shipping the completed wafers to assembly vendors overseas.

By the time GaAs wafers complete frontside final test, they have already been through close to 300 frontside process steps. Each has the potential of adding a small amount of stress to the wafer. At final test, they are decidedly weaker than when they started. During frontside operations, it is possible to isolate and remedy the cause of the stress, since most times wafers will break at or immediately after the offending step, and it is easy to check for tool commonalities or other contributing factors.

Many stresses are at play during the backside process sequence, but their impact is rarely observable until the wafers are demounted from the sapphires, which makes it difficult to pinpoint a specific cause. A small, but not insignificant, portion of these wafers are found broken at demount. These pieces are mounted on separate saw frames, diced, and shipped. This can have a significant impact on throughput especially during times of high production volumes.

A team including process engineers and technicians, equipment engineers, production, and R&M personnel was set up with a mandate to reduce wafer breakage (and consequently partial wafers shipped). The team made some important discoveries about the causes of wafer breakage, and the strong interaction among the many factors at play, and succeeded in achieving historic low levels of breakage.

APPROACH

The team started with a detailed analysis of the entire backside process operations, and then proceeded to delve into the details of each operation studying individual steps in detail to make it easier to identify all possible sources of stress on the wafer. A typical backside process flow in shown in figure 1, while a sample individual operation breakdown is shown in figure 2.

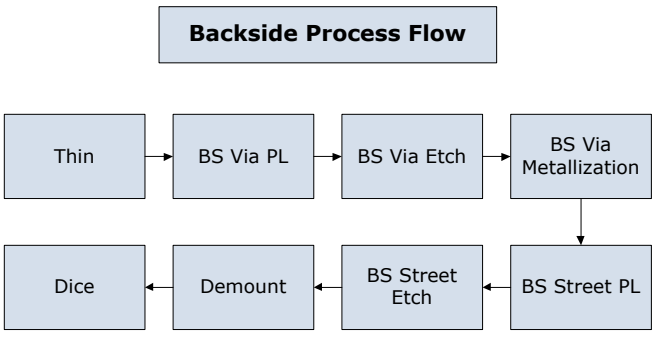

Figure 1, overview of backside process flow sequence

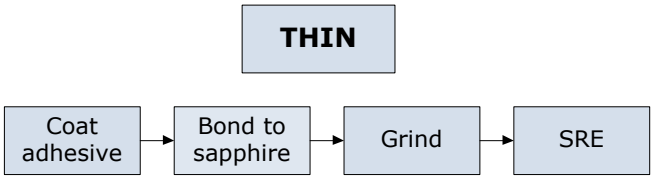

Figure 2, Detail of the thinning operation

From this basic flow, the team constructed a fishbone diagram as an additional diagnostic tool; a slimmed down and truncated version of which is shown in figure 3.

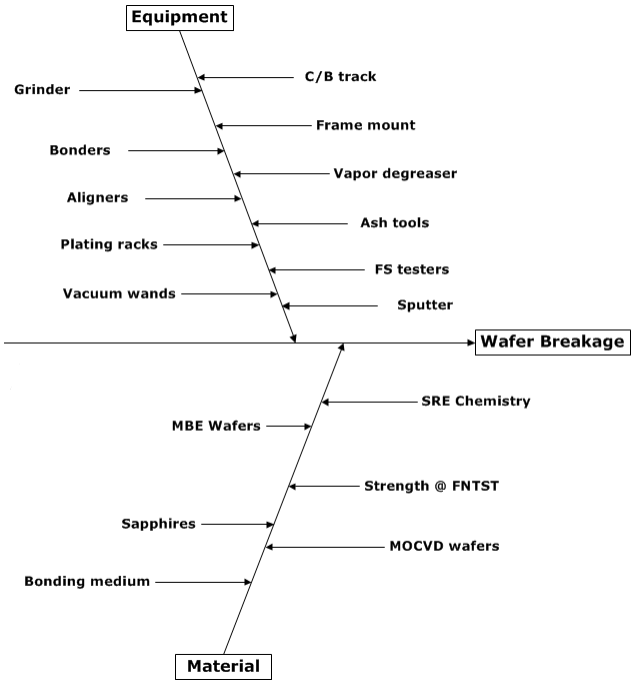

Figure 3, partial fishbone diagram to reduce wafer breakage

The team also employed area audits by select groups. These groups consisted of representatives from the various stakeholders. Each group audited an operational area that was not under its direct responsibility. This approach was intended to bring a set of fresh eyes to that area, and allow for an unencumbered critique of processes, equipment, and procedures. The team carefully reviewed the outcome of these audits, and implemented changes as necessary.

RESULTS

Final glassivation thickness was determined to be an important factor in wafer breakage; products that had thicker silicon nitride tended to have higher breakage rate (figure 4). This is due to the increased film stress which is reflected in wafer bow. Changing the glassivation thickness is a difficult process that may require customer approval, so we set out to attempt to reduce wafer bow. Here we focused on the stress relief etch chemistry and whether an alternate chemistry would have an impact on wafer bow, and thus reduce breakage. It did (figure 5). Changing the SRE chemistry led to a 25% reduction in wafer bow, which translated to a reduction in broken wafers at demount. It also reduced the number of wafers broken after demount as higher stressed wafer tended to break more frequently during transportation or saw frame mounting.

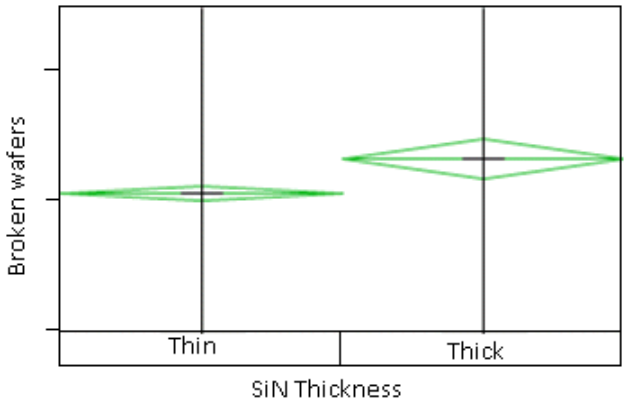

Figure 4, Effect of final SiN glassivation thickness on wafer breakage

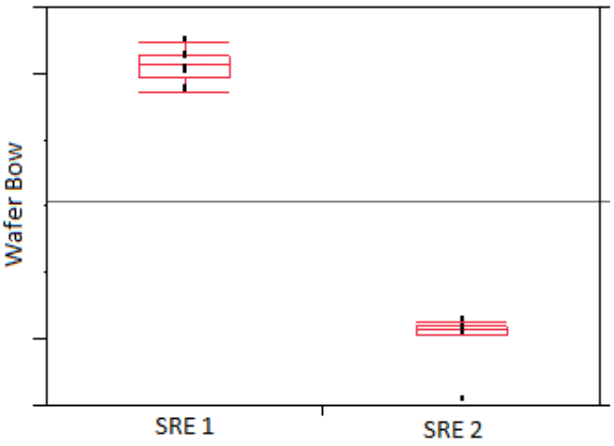

Figure 5, Effect of SRE solution on wafer bow

In addition to internal wafer stress, external wafer damage can cause breakage. There are many places where this could happen. We started with the grinding operation and investigated tool parameters such as downward speed and amount of material removed during the fine grinding step. None had a significant impact. However, sometimes debris on the porous ceramic end effector that handles the thinned wafers will cause a crack in the wafer that will break later. This source of breakage was random. Working with our grinding equipment supplier, we were able to design and install new end effectors that do not contact the thinned wafer at all.

Aligner "flags" were another source of external damage. In addition to a stress point at that location, a mechanical imprint from these flags on the via etch photoresist can lead to a hole being etched through the wafer at the subsequent etch operation. This issue was remedied by moving the flags off the wafer and onto the sapphire during the alignment sequence. Also in the photolithography area, mask defects or scratches can lead to similar issues. Careful inspection of the wafers can usually identify these issues because of their repeatable location on the wafer, since this is the only area in the backside where wafers are oriented.

Inspection of broken wafers revealed that the majority of the breaks originated at a plating contact point, of which there are 4 on each wafer. An effort to redesign the plating rack is underway with an emphasis on reducing the impact and damage caused by the plating contact. In the meantime, we have attempted many different "fixes' to reduce the impact of the existing plating rack. The effect of these "fixes' was minimal. Something else was at play here that we needed to understand.

Careful inspection and observation proved that there is no substitute for time spent in the fab looking at product. This is where we observed that some wafers were "wavy" around the perimeter prior to the plating operation. Subsequent height measurements showed that some wafers were significantly higher at the edge than they were at the center. They were flat when bonded, but that was no longer the case just prior to plating. The bonding medium was wrinkled around the perimeter of the wafer and caused the wafer to lift slightly from the sapphire. We hypothesized that the elevated temperature at seed layer sputter deposition was the direct cause. These wafers were prime candidates to break, as any pressure from the plating contact is enough for a break to initiate, and that is precisely where the wafer will come apart at demount.

We worked with our bonding medium supplier toward a solution that required a fairly simple modification of its composition. We hypothesized that such a modification would make it more resistant to our process and environmental conditions in the fab. Our supplier provided us with a sample for evaluation. Figure 6 shows the impact of this new material on maintaining a uniform stack height (this is the total sum of the sapphire, wafer, and bonding medium thickness) as a function of process temperature and applied thickness. It is clear that this modified material is significantly more uniform at higher temperatures and more robust relative to its applied thickness.

The bonding medium supplier agreed to commercialize this modified product, and supply it to RFMD to replace the one we were currently using. We have seen a significant drop in broken wafers after we implemented this change.

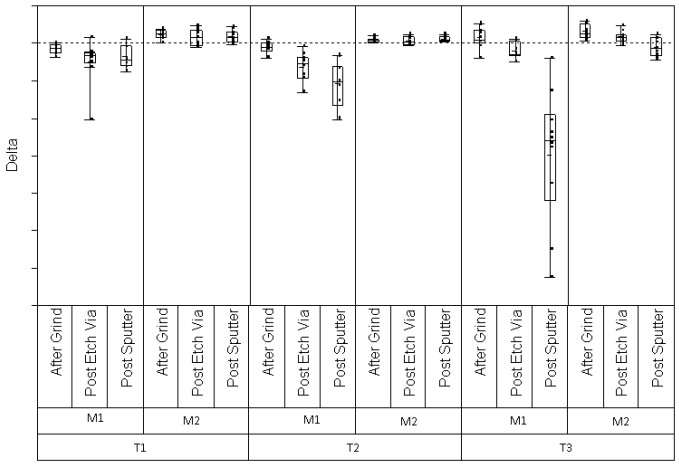

Figure 6, Effect of bonding material composition and thickness on wafer flatness at various steps.

For the past 18 months we have diligently worked toward identifying every existing source of wafer breakage, and sought a solution. These ranged from equipment handling issues, to intensive and continuous operator training. The results have been encouraging as can be seen in figure 7. This figure also shows that we remain prone to periodic fluctuations in broken wafers, and understanding its causes will be important in realizing additional gains.

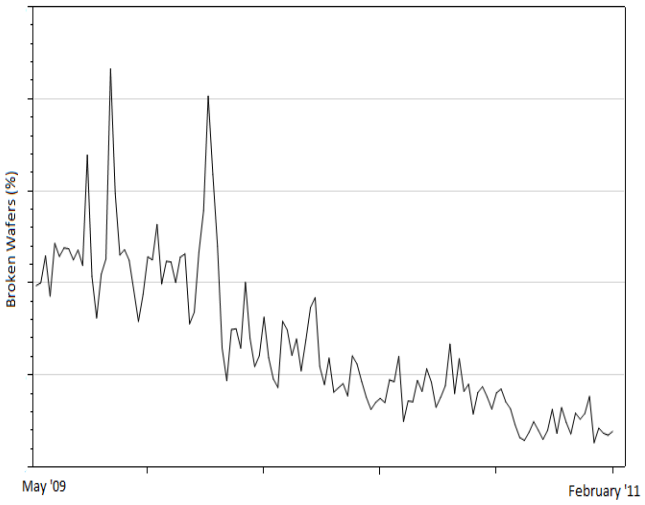

Figure 7, Broken wafer trend over an 18 month period since this project began

We have evaluated some innovative modifications to our current processes, some of which have shown promise and will undergo extensive testing over the next few months. New equipment configurations are also being considered and evaluated.

CONCLUSIONS

Backside operations are an integral and important part of a wafer fab, and any loss this far into the process is very expensive since most of the resources have already been invested to get the wafer to this point.

By using all available analytical tools and good old fashioned observation, we have been able to identify major contributors to thinned wafer breakage, and implement the needed solutions to minimize it.

To reduce wafer breakage we investigated every aspect of the process flow, and found that multiple factors have a significant impact, and there is a strong interaction among some of them.

ACKNOWLEDGEMENTS

The author would like to thank all the dedicated RFMD personnel that worked on and assisted with this project. Their contributions were vital and will continue to be an important piece in maintaining and improving the backside process.

ACRONYMS

GaAs	Gallium Arsenide
R&M	Repair and Maintenance
SRE	Stress Relief Etch