

The Demonstration of Enhancement/Depletion-Mode pHEMT Technology with Optimized E-mode Characteristics for Better Yield

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Abstract

E/D pHEMT technology has become important for wireless switch and LNA applications. To meet the requirements of both low cost and tight E-mode pHEMT threshold voltage control, one has to compensate for natural variation of the epitaxial layer growth. WIN has developed a manufacturable gate sinking method to achieve tight control of E-mode pHEMT pinch-off voltage of commercially supplied epitaxial E/D material.

INTRODUCTION

Because of the Desktop/Handset wireless communication market keep growing for the passing years, demands of foundry services that can provide low cost, high yield, low-noise amplifier (LNA) that fully integrated with RF switch or logic control function also growing. WIN PD50-01 technology [1] uses the well established D-mode pHEMT switch epitaxial layer structure and adds an E-mode pHEMT device to it using Pt for gate metal sinking. The advantage of this approach is that all the designs and products based on the production switch process can take advantage of the new PD50-01 technology (Table 1) as well. In general metal sinking process itself is a complicated and hard to control approach if we compare with epitaxy design engineering [2], but we believe it also have the potential to result a more consistent and repeatable noise performance, Fig 1, for customers naturally, that is because gate depletion area is deeper into semiconductor and far away from surface that may affect the device performance. The other benefit of sinking gate approach is that technically the way of process control can be easily applied into any other baseline released D-mode pHEMT technology without involving any EPI re-design no matter what the gate length dimension it is. We believe the flexibility of process should benefit most customers who are looking for an instant integration solution for their designs.

DEVICE STRUCTURES AND FABRICATION

pHEMT MMICs consist of an epitaxial structure grown on top of a GaAs substrate to result the active device and bulk resistors, as well as numerous passive elements formed

in the fabrication process. The structure of the epitaxy consisted of a thin, undoped InGaAs channel layer sandwiched between Si delta-doped layers that provides carriers to the channel. Undoped AlGaAs spacer layers were grown between the channel layer and the Si delta-doped layers. An AlGaAs Schottky layer was placed on top of the upper spacer layer.

TABLE 1
THE PD50-01 CHARACTERISTICS SUMMARY TABLE

WIN PD50-01 0.5μm InGaAs pHEMT Enhancement/ Depletion-Mode Technology	
MASK Layer	13 (11 frontside layer ; 2 backside layer)
Connection MET	2 metal layer
Resistance	50, 150 , 300(optional) ohm/□
Capacitance	300, 600, 900 pf/mm ²
Recess Number	Single
EPI material	The same with WIN P550-01 Switch Technology
D-mode Process	Compatible with WIN P550-01 Switch Technology
E-mode Process	Metal sinking to result the Enhancement-mode device

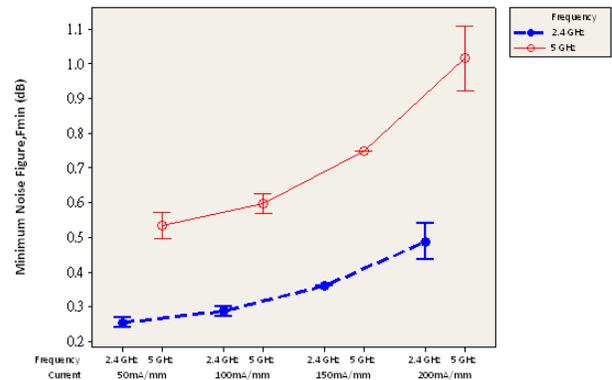


Figure 1: The VDS=3.5V 2.4&5GHz Fmin data

For device fabrication, ohmic pattern was defined by optical lithography and Au/Ge/Ni/Au/Ti metals were evaporated in the contact regions in order to have good ohmic contact. Then, ohmic contacts were annealed by RTP. In order to avoid side-wall gate leakage, the ion-implant isolation was applied to device isolation. Compared to isolation by chemical etching, ion-implant also provides a flat surface, which is good for high gate yield. Both D-mode pHEMTs and E-mode pHEMTs are with 0.5um gate length

defined by optical lithography and single recess, but each mode was processed respectively. Due to metal sinking process was used to result enhancement mode, in order to avoid gate metal sinking simultaneously, E-mode devices need to process before D-mode devices. The E-mode gate metal scheme was deposited from bottom with the sequence of Pt/Ti/Pt/Au and metal sinking by RTP. Regarding the passive components, we provide 50 ohm/□ TaN thin film resistor and two metal inter-connection layers, one is 1um and the other is 2um gold thickness. With low-k polyimide dielectric layer covered by thick compressive final protect SiN for humidity protection. Finally, the substrate will be thinned down to 4-mil thickness with 4-um plating gold backside via process.

RESULTS AND DISCUSSIONS

The natural of molecular beam epitaxy (MBE) growth EPI will result certain level doping distribution within each wafer, therefore, parts of E-mode device performance variation like pinch-off voltage will be due to epitaxy doping distribution itself and at the same time the sinking metal thickness control will also contribute the device performance variation further more. The improvement of epitaxy growth no matter for within wafer uniformity or run to run consistency means the higher epitaxy cost, normally there is no quick win solution and that is why we focus on the process study and optimization. According to wafer range of D-mode pinch-off voltage accumulated data, Fig 3, we can see for each single 6-inch wafer, the range of D-mode pinch-off voltage across wafer caused by epitaxy growth is around 0.12V. Because the process design, the D-mode and E-mode device gate metal are deposited on the same epitaxy layer, the intrinsic variation of E-mode pinch-off voltage should be similar with D-mode value. Due to this E-mode pinch-off voltage within wafer variation we often see numbers of wafer suffer high yield loss only through the basic 100% DC function test, like operation current for E-mode device of LNA. The thickness control of bottom Pt layer was important and critical to get extremely tight control of E-mode pinch-off voltage to minimize the 100% DC yield loss. By the study of E-mode gate evaporation tool and intrinsic epitaxy doping variation, combining the in-line tacking and wafer handling optimization, we minimize the E-mode device within each wafer and improve the long term product performance consistency. With this help of process optimization we can reduce the range of E-mode pinch-off voltage across wafer from 0.11V to 0.08V, Fig 4, and maintain long term E-mode pinch-off voltage within a very tight distribution, Fig 5, with superb 100% DC test average yield over 98% at same period of time.

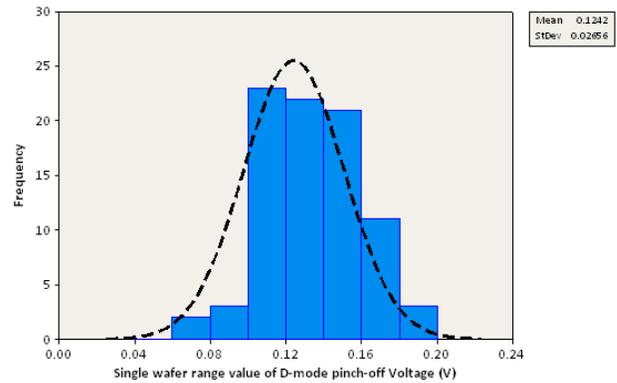


Figure 3: The range of single wafer D-mode pinch-off voltage

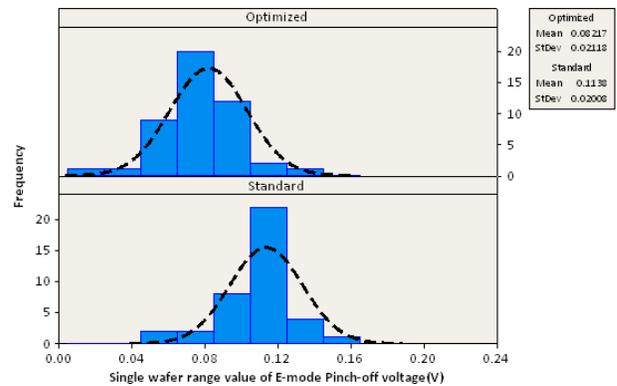


Figure 4: The range comparison of single wafer E-mode pinch-off voltage

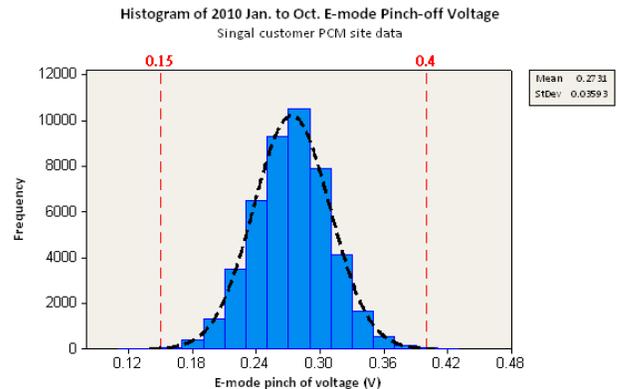


Figure 5: Long term E-mode pinch-off voltage distribution

CONCLUSIONS

WIN semiconductor corp. developed the Enhancement /Depletion-mode pHEMT technology (PD50-01) to match market requirement, with only epitaxy intrinsic doping within or run to run wafer variation will result numbers of wafer suffer high yield loss. We demonstrate the extremely

high 100% DC long term yield by optimizing the metal evaporation process and wafer handling methodology.

REFERENCES

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ACRONYMS

pHEMTs: pseudomorphic High Electron Mobility Transistors
D-mode: Depletion mode
E-mode: Enhancement mode
MMICs: Monolithic Microwave Integrated Circuits
EPI: EPItaxy
RTP: Rapid Thermal Processing
MBE: Molecular Beam Epitaxy