# Role of Buffer Layers of High Power GaAs MESFETs for Higher Output Power

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**Keywords: GaAs, MESFET, PA, High output power, Buffer**

## ABSTRACT

**For the high power GaAs MESFETs with high efficiency and high output power, it is necessary to improve the performance of epitaxial buffer layer. It is found that electrons flow at near the buffer layer and the saturation performance under high power is very effective. Based on this idea, high performance buffer layer with periodic stacked GaAs/AlGaAs layer is developed and successfully improved high power FET performance.**

## INTRODUCTION

The GaAs MESFETs have been used for the high power amplifiers for base stations and CATV systems. For these applications, a very simple structure using n-GaAs channel layer with AlGaAs buffer layer has been used. Sometimes degradation with RF performance has been observed. The degradation was closely dependent on production method while DC performance had no effect. It has been known that buffer structure affect the RF performance, but the mechanism of this degradation and the method of optimization were not well understood.

In this paper, we will theoretically and experimentally explain the effects of buffer layer on the performance of MESFET PA, and develop a high performance MESFET for high power amplifiers by using optimized buffer structures.

## HOW THE BUFFER AFFECTS TO THE PA PERFORMANCE

The impurities that exist as donor or acceptor at the epi/sub interface are known to affect PA performance. This is because these impurities make high density donor or acceptor level and generate free electrons, thus affecting the electron flow due to change in electric field. This is big issue for MBE and MOVPE growth, but we developed a novel method of having high purity epi/sub interface by carrying out a special treatment before epitaxial growth, and the reduction of impurities [1, 2].

The roll of buffer structure is discussed from the viewpoint of transistor operation. The typical I-V curves of FET are shown in Fig. 1. The small signal operation like class A has the operating point as shown in point (a) in the I-V curves and the depletion layer reaches only to middle of channel layer shown in Fig. 1(a). The performance of small signal transistor is more or less decided by the quality of channel layer because the operational bias small and the depletion layer changes only in channel layer. On the other hand, high power operation such as class B or C uses negatively higher Vg as operating point, and the depletion layer goes deep into near the buffer layer like Fig. 1(b) (this corresponds point (b) in I-V curves). Thus electrons flow near the interface of channel and buffer. If the quality of this interface is poor or if there are some impurities in the buffer layer, electron flow degrades and results in a noise in RF signal as well as lower output and linearity of PA as shown in Fig. 2. Hence it is imperative to understand how electrons flow near the buffer layer. If the Vg is biased towards more negative direction from operating point (b), the depletion layer will extend into buffer layer as shown in Fig 1(c) (point (c) in I-V curve). In ideal case, electrons should not flow. If there is a leakage current in the buffer layer, it will contribute to degradation in RF signal in Fig. 2 and cause lower output power and lower efficiency. Thus it is important to know the leakage is in the buffer layer.

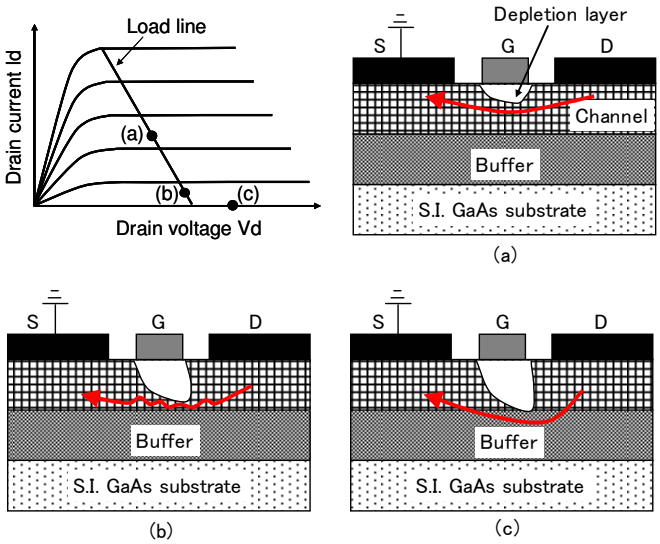


Fig. 1 Typical I-V characteristics of FET and schematic image of electron flow in each Vg condition. (a) and (b) are operating points of class A and B, respectively. At (c), depletion layer reached to buffer layer.

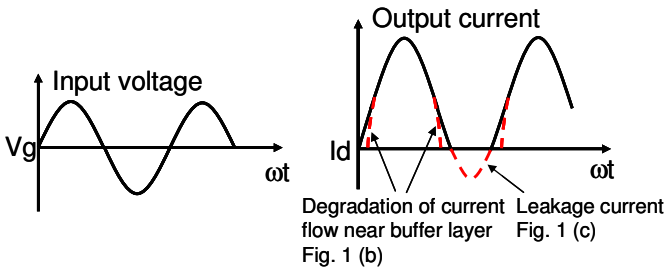


Fig. 2 Schematic images of input and output. Broken lines in output current show the noise elements.

The criteria for high RF performance in power transistors are:

(1) to reduce impurities at epi/sub interface
(2) to improve the electron flow at the channel layer near the buffer region
(3) to decrease leakage current at buffer layer as shown in Fig. 3.

We have achieved (1) and, the effects of (2) and (3) were experimentally investigated.

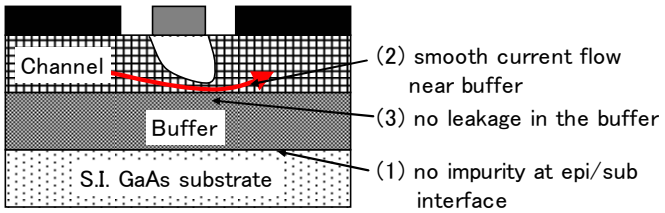


Fig. 3 The important features to improve high voltage performance.

## EXPERIMENTS

In order to understand the effect of buffer layer on adjacent layers, different buffer structures were grown in MOVPE shown in Fig. 3. Same MESFETs with n-type GaAs channel of 1E17cm-3 were used for all different buffer structures. The thickness of buffer layer at 300nm n-Al0.20GaAs single layer on i-GaAs, shown in Fig. 4(a), was used as standard. To understand the effect of Al concentration, samples 1 and 2 had higher Al composition (0.28 and 0.40, respectively). At higher Al concentration in AlGaAs, the higher the hetero barrier, and this is known to prevent leakage current. Sample 3 had thinner AlGaAs buffer to understand the effect of buffer thickness. In sample 4, multiple GaAs/AlGaAs hetero junctions were used to know the effect of multiple hetero barriers as shown in Fig. 4(b). For this layer, 3 pairs of 50nm-i-Al0.20GaAs/50nm-i-GaAs were grown and maintaining the total thickness the same as the standard. The performances of these samples were measured utilizing transistor structure. The gate length of this transistor was 0.8μm and the gate width was 200μm. Al/Mo and AuGe/Ni/Au were used as gate metal and schottky metal, respectively.

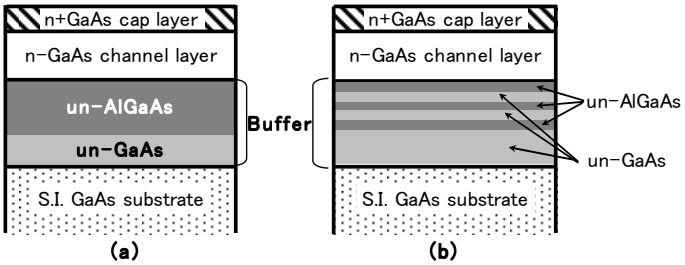


Fig. 4 MESFET epitaxial structure with (a) single AlGaAs buffer, (b) multiple AlGaAs/GaAs buffer.

| | | Standard | Sample 1 | Sample 2 | Sample 3 | Sample 4 |
|---|---|---|---|---|---|---|
| i-AlGaAs | Thickness (nm) | 300 | | | 50 | multi layer |
| | Al Conposition | 0.20 | 0.28 | 0.40 | | |
| i-GaAs | Thickness (nm) | 200 | | | - | |
| S.I. Sub | | H. C. | | | | |

Table 1 Buffer structure of each sample. Blank boxes are same as standard. "-" means not applicable. "Multi layer" is 3 pairs of 50nm i-GaAs and 50nm i-AlGaAs (Al=0.20).

To understand the effect of (2) and (3) in Fig. 3, we measured the properties of delta Gm and delta Id. The Delta Gm is defined as the difference of Gm at Vth (Vth is defined as the voltage when the Id becomes 20μA at Vd=3V) and at Vth+0.3V as shown in Fig. 5(a). This shows how smooth the current flows near the buffer ((2) of Fig. 3). The delta Id is defined as the difference of Id at the Vd=3V and 11V (Vg is set to have Id=200μA at Vd=3V) as shown Fig. 5(b). This can help determine how large the leakage current is through the buffer ((3) of Fig. 3). Therefore, the good buffer structure should have large delta Gm and small delta Id.

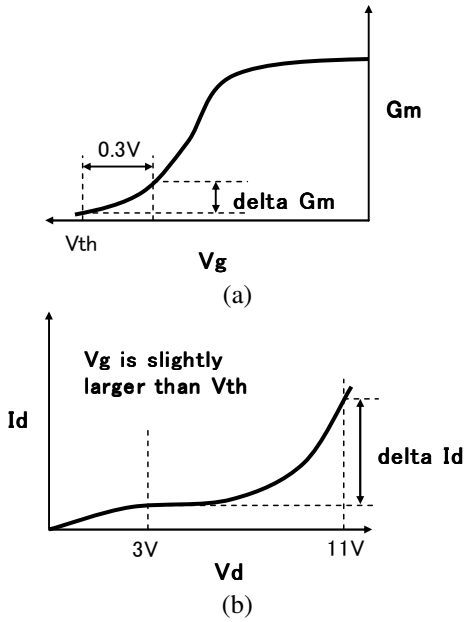


Fig. 5 Definitions of (a) delta Gm and (b) delta Id. (a) quantifies the electron flow near the buffer and (b) quantifies the leakage current in buffer.

## RESULTS AND DISCUSSIONS

The results of delta Gm and delta Id of each sample is plotted in Fig. 6. Even though the same n-GaAs channel layer thickness was used, the results show large differences between different buffer structures. The delta Gm was smaller with higher Al concentration with x=0.4 (sample 2) compared to other samples where no noticeable changes were observed from the standard. As for the delta Id, there was no difference in Id at Vd=3V, but a large difference was observed in Vd=11V. The increase of Al concentration (sample 1 and 2) and the use of multiple layer hetero junction (sample 4) have significantly improved the performance (low delta Id). Sample 3 with thinner AlGaAs showed increase in delta Id.

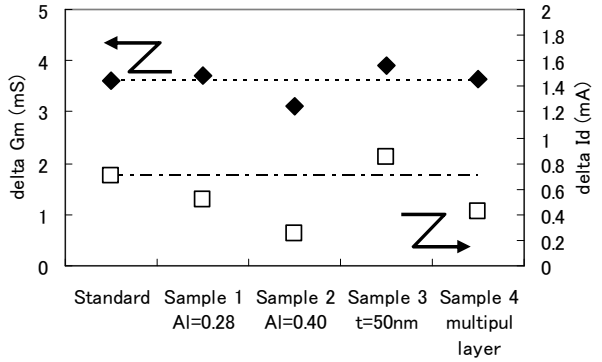


Fig. 6 Results of delta Gm and delta Id in each samples.

To understand the delta Gm change by the difference of Al concentration especially in Al=0.40, we evaluated crystal property utilizing Hall measurement with wet etching. This can provide the information near the buffer layer by the progress of etching. The electron mobility vs. sheet carrier concentration (Ns) was plotted for three different thicknesses in Fig. 7. We found the difference of delta Gm and electron mobility obtained in this experiment had close relationship. Sample 1 had almost the same mobility compared to standard. However, the mobility of sample 2 decreased as sheet carrier concentration decreased, thus the difference compared to the standard increased at lower region while no differences were observed at higher region. Mainly, mobility is affected by the impurity level that results in ion scattering. It is well known that AlGaAs with high Al concentration easily absorbs oxygen. Therefore, to lessen the oxygen absorption, minimizing the Al concentration level is the key to avoiding deep level phenomenon.

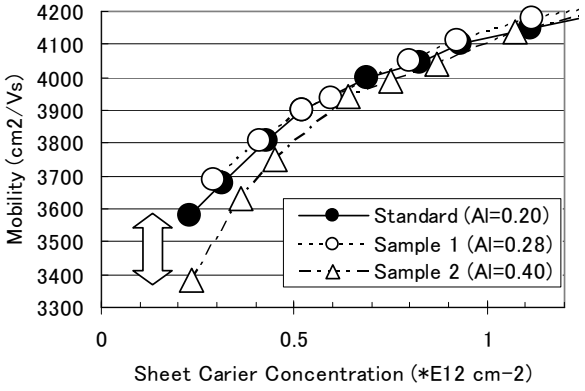


Fig. 7 Results of Hall measurement. Hall measurement and wet etching were repeated to know depth dependence of mobility.

From the results of Fig.6, we found higher Al concentration was effective to improve leakage current due to the increase of hetero barrier as expected. Also it was found that simple AlGaAs buffer needs some level of thickness (around 300nm) to prevent leakage. For the multiple hetero junction structure, the performance improved even though it has same Al concentration and same total thickness with standard. We carried out a simulation utilizing finite elemental analysis to determine the multiple layer buffer improvement of delta Id. We calculated drain current under the condition of high negative gate voltage (Vg=-4V) with value range from 0V to 18V. We assumed this Id as leakage current through buffer layer. It was found that the leakage current of multiple layer buffer is obviously lower than the single layer buffer as shown in Fig. 8. This result had close relationship with the difference of delta Id. Also we found from the simulation that most leakage current flows via GaAs substrate through the buffer layer under the high Vg and Vd condition as shown in Fig. 9. The leakage current flows downward from source electrode to substrate through the buffer layer, and flows through bulk substrate, then flows upward toward drain electrode through buffer layer (Fig. 9(a)). Therefore, leakage current has to pass the buffer twice to reach drain electrode from source. Multiple layer buffer has several hetero junctions where current has to pass the hetero barrier several times as shown in Fig. 9(b), thus gradually decreasing the current density.

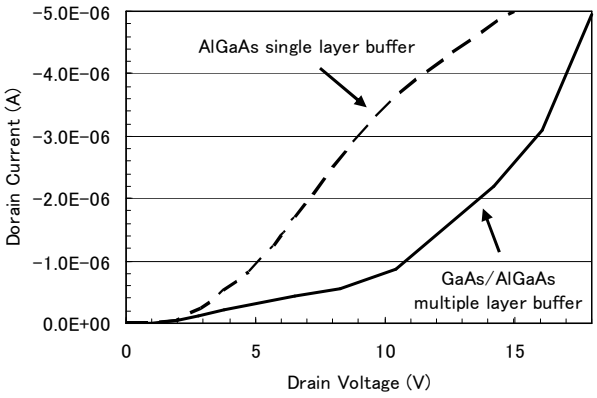


Fig. 8 Comparison of leakage current between AlGaAs single layer and i-GaAs/i-AlGaAs multiple layer buffer.

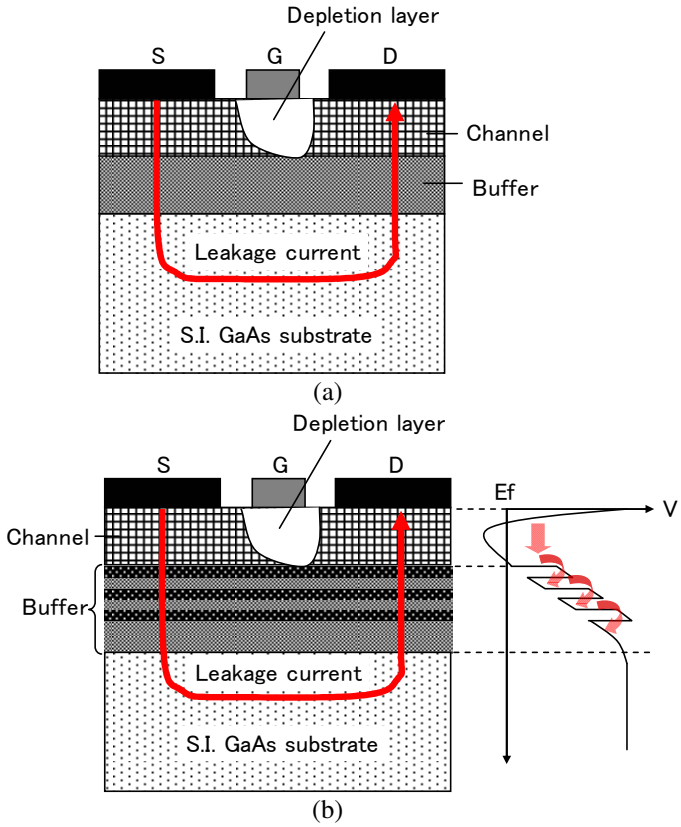


Fig. 9 Schematic image of (a) leakage current flow through buffer layer and (b) the leakage current flow of multiple buffer.

Based on these results, we were able to understand and implement buffer structure design to have smooth electron flow near buffer layer and low leakage current. The proper Al concentration should be between 0.20 and 0.40, and multiple hetero junction buffer is more effective than single layer. By using these design rules, we were able to optimize the buffer structure with multiple layers and measured the output power as shown in Fig. 10. We were able to gain 20% higher output power compared to previous standard structure with single AlGaAs buffer layer. As a result, we conclude that the buffer design had major affects on high power transistor.

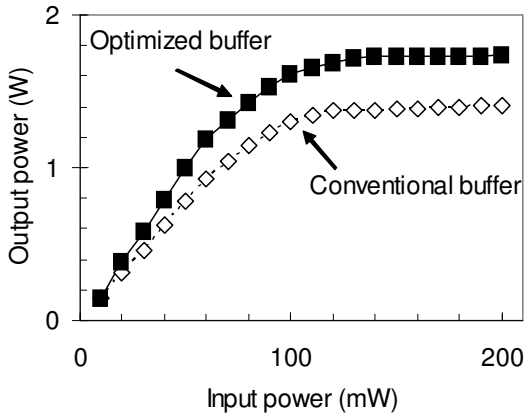


Fig. 10 Comparison of MESFET output power between conventional and optimized buffer.

## CONCLUSIONS

A MESFET structure for high power application needs not only high quality channel but also optimized buffer layer design. The key factors for high PA performance are less impurity in epi/sub interface, smooth electron flow near the buffer layer and low leakage current at buffer layer. We found the buffer structure with proper Al concentration and multiple hetero junctions are effective. Based on these ideas, we successfully achieved 20% higher output power by utilizing optimum buffer design.

## REFERENCES

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## ACKNOWLEDGEMENT

Authors appreciate Gene Kohara of Marubeni America for his kind support.

## ACRONYMS

(Al)GaAs : (Aluminum) Gallium Arsenide
MESFET: Metal Semiconductor Field Effect Transistor
PA: Power Amplifier
CATV: Cable Television
RF : Radio Frequency
DC : Direct Current
MBE : Molecular Beam Epitaxy
MOVPE: Metal Organic Vapor Phase Epitaxy