SESSION 8a: PROCESS III- LITHOGRAPHY/BCB

Chair: Chris Yousey, *MicroLink Devices, Inc*

Presentations in this section, from several leading GaAs IC manufacturers, describe a range of practical challenges associated with device lithography, planarization and the novel solutions that were developed to improve process yield and robustness.

The first paper of the session from Skyworks Solutions presents a new method to create sloped resist profiles by exposing with patterns that incorporate microstructures below the stepper optical resolution limit. This enables partial exposure of the resist around the designed features and localized control over the development rate. Sloped resist profiles are an important method in device fabrication to minimize abrupt step height changes. This presentation discusses the advantages of the new technique compared with conventional approaches such as thermal reflow or exposure defocusing.

The following paper from TriQuint Semiconductor presents a new trilayer resist electron beam lithography process used to form T-gates for GaAs pHEMT devices. The new process improves process yield by reducing metal liftoff “stringer” defects encountered when using the conventional bilayer resist. Cross-sectional FIB-SEM images clarify the mechanism for defect formation, and DC and final visual yield data validate the process improvements.

Next TriQuint Semiconductor presents a critical process issue encountered when using photo-definable BCB to encapsulate HBT and pHEMT GaAs MMIC circuits. Intermittent wrinkling of the BCB dielectric was solved through a DOE that clarified proper exposure, development and baking parameters.

The final paper from Avago Technologies discusses the challenges of using BCB to planarize over topologies with widely varying pattern density. Local variations in BCB thickness can lead to shorts as well as incomplete metal via formation. Optical profiler measurements of BCB film thickness over a complex circuit structure are compared with predictions from a model that is incorporated into a design-rule checker. Electrical test structures are also described that are used to characterize the process limitations.