Electrical, Thermal, Reliability and Cost Considerations for Millimeter-Wave Surface Mount Packages

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Abstract

Package electrical effects grow in significance with frequency, and must be factored into chip design early in the design cycle. Similarly, the thermal properties of the package must be taken into account for higher power parts like amplifiers. Package choice is also determined by reliability requirements and cost. These factors combine to determine the ultimate suitability of package types and their performance envelopes. This paper discusses the trade-offs in package design and technology selection, from standard QFN through to custom laminate packages.

INTRODUCTION

In recent years there has been growing interest in surface mount packages for millimeter-wave components. The replacement of chip-and-wire assembly with pick-and-place technology has enabled aggressive cost reduction in price sensitive applications and simplified board or module designs. M/A-COM Technology Solutions has successfully used overmolded plastic QFN packaging for high performance applications to 40 GHz, and cavity laminate packaging to 43.5 GHz. Detailed thermal modeling of the package paddle, and rigorous electrical modeling of the package transition from die though bond wires to the application board are required, so that appropriate active region design and matching limitations can be designed in and optimized for. Furthermore, cost margin and reliability requirements to meet customer needs also determine the package options available, typically putting significant constraints on what can be achieved in terms of transition loss, temperature rise and moisture sensitivity.

ELECTRICAL PERFORMANCE

Standard plastic overmolded QFN packages deteriorate in electrical performance above 30 GHz, though with careful die design they have been used to 40 GHz (See Fig 1(a) for a 2.4 mm die in a 4×4 mm QFN). Superior performance can be obtained with a cavity laminate with a custom design. Fig 1(b) shows performance for a 2.4 mm die in a 5×5 mm custom laminate package. The laminate material is RO4350B. This package incorporates a solid copper pedestal for the die and a matching network on the top side of the laminate. The laminate is, however, more costly than the QFN and requires a separate lid and lid attach phase in production.

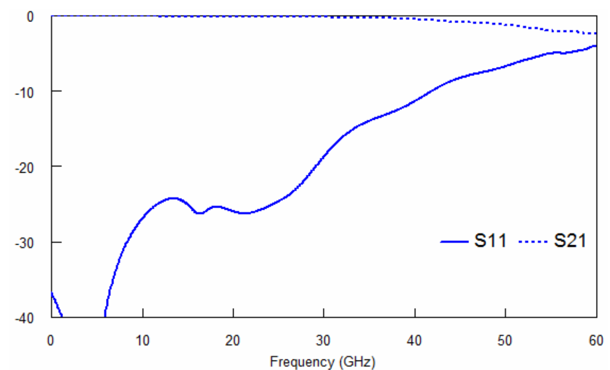

Fig 1(a). Transition for a 2.4mm die in a 4×4 PQFN package

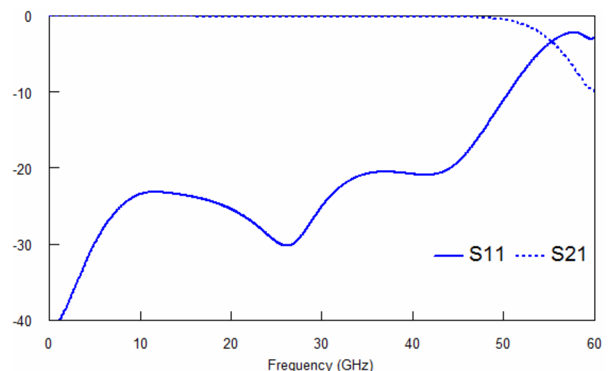

Fig 1(b). Transition for a 2.4mm die in a custom 5×5 Cavity Laminate Package

Detailed comparison of the measured and modeled transition performance for various package types up to 60 GHz will be presented in the final paper.

THERMAL PERFORMANCE

The design of power amplifiers is usually thermally limited by the temperature rise across the semiconductor die, die attach epoxy, package materials, solder layer and printed circuit board. For most GaAs technologies the junction temperature must be below 150°C so that degradation due to thermally induced wear-out modes is insignificant. Packages in which the die is attached to a solid copper leadframe, pedestal or coin offer the best thermal environment with the package contributing 5 to 20% of the total thermal resistance for high power devices. However, such packages are expensive to manufacture because they typically require milling and insertion of a coin or lengthy pedestal plating. A cheaper alternative are laminate packages with a via array underneath the die. Via arrays have anisotropic thermal properties that are strongly influenced by the density of vias and via fill material. The most dense array of copper-filled vias has approximately 25% copper by area in cross section and its anisotropic thermal conductivity results in poor lateral heat spreading inside the package. Consequently laminate packages with via arrays under the die have a thermal resistance three to four times higher than a solid copper pedestal. In such cases the thermal resistance of the laminate package can be a very significant part of the overall temperature rise and may necessitate larger die size or sub-optimal DC bias point.

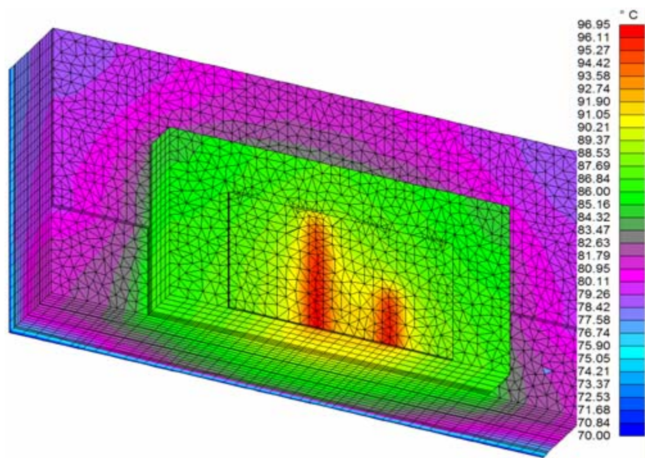

Fig 2. Thermal model of power amplifier die in a 7×7 PQFN package (epoxy/die junction layer shown)

Finite-element thermal models of different package types will be presented and discussed in the final paper. Trade-offs in the design of packages for high power applications will be discussed.