Manufacturing of Cu-pillar Bump for III-V MMIC Thermal Management

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Cu-pillar bump manufacture technology applied on III-V MMIC thermal management is reported. IBM C4 technology has been used in high volume production on CMOS wafers for decades. In addition to smaller real estate on PCB, when coupled with the corresponding flipchip packaging structures, better performance in both thermal and electrical characteristics could be expected from bumped chips especially when the application powers or frequencies are higher. When coping with higher thermal density and flexible thermal source distribution, Cu-pillar bump design outclasses the solder bump structure which is prevailing in CMOS community. However there were several potential obstacles for the manufacturing of Cu-pillar bump structures on GaAs wafers, including the brittleness of the substrates, thermal bar design induced extra bump coplanarity, and the productivity problem due to low copper deposition rate. Approaches to solve these potential issues are addressed in the report.

Thermal bar design induced extra bump height difference

When there is only one bump size appearing in the wafer, in-wafer coplanarity can reach <5% to reduce some potential difficulties encountered during wafer probing and flipchip assembly, figure 1 shows the bump height distribution on a test vehicle.

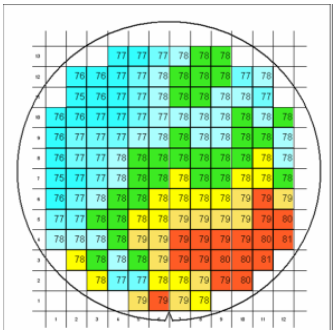

Figure 1. Bump height distribution in the wafer. Good in-wafer coplanarity can be achieved when the bump size is the same across the wafer.

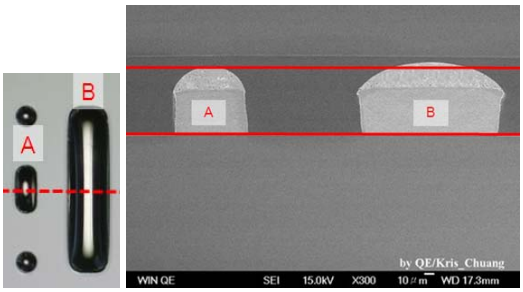

Figure 2. Cross-section shows different bump heights can be expected from different bump sizes although they are in the same chip. Larger bumps tend to have higher bump heights.

When the thermal bar designed is included in the chip, the aspect ratios of the photoresist openings will be different in the same chip and consequently it makes the boundary layer thicknesses along the surface of cathode vary in the same chip and result in different metal deposition rates. According to measured bump height data, coplanarity sometimes become worse after solder reflow and it could

make flipchip assembly difficult if Cu-pillar bump's in-chip coplanarity become too large. One quick way to avoid this in-chip coplanarity problem is to arrange solder reflow to take place after flipchip die bonding step. However it will not be convenient to do after-bumping probing without reflow process first. To solve this in-chip coplanarity problem, one additional step is successfully adopted to control the volume of solder deposition to minimize the bump height difference between thermal bars and normal bumps. The results shows that 5% in-chip coplanarity is possible even when there are several different bump sizes.

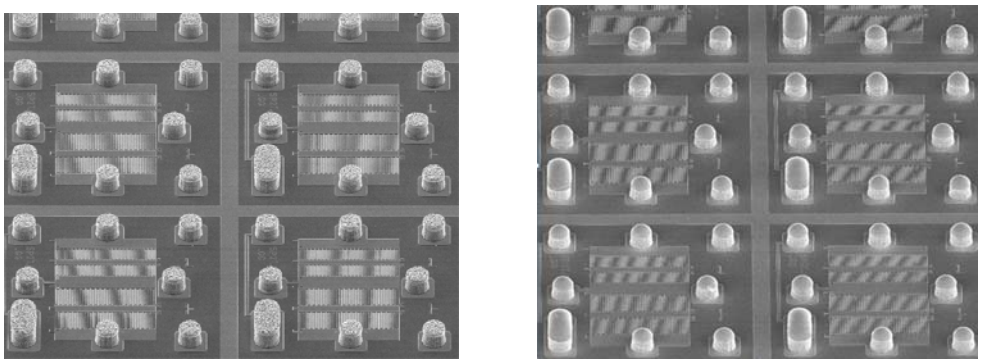

Figure 3. Plated Cu-pillar bump before reflow (left hand side) and after reflow (right hand side). It used to take after-reflow bumps to do flipchip assembly, but sometimes before-reflow bumps are used to reduce in-chip coplanarity when doing flipchip assembly.

Brittleness of substrate

Due to its brittleness, bumping process on GaAs wafers experienced breakage rates as high as 15-25% at the beginning stage when outsourcing to some facilities which are mature and familiar to bumping process on Si substrates. Although it is reduced later, the breakage rate is still higher than its counterpart for Si wafers. It is believed that the process tool design and the agitation during long distance shipping are the major factors for wafer breakage. With selected tools set and modified process, the wafer breakage rate is well controlled below 1% when MMIC process & bump process are completed in the same fab site.

Deposition rate

With some matured copper electroplating chemicals in the market, it will take 40-60 minutes to finish the copper deposition for Cu-pillar bump to receive both good grain size and low dorming. At this deposition rate, only 600 wafers/ month can be expected from one copper plating cup, and consequently the cost of Cu-pillar bump will be increased significantly. After considering factors like quality, cost, throughput, and chemical management etc, a decent chemical is found to meet all the requirements and suitable for high volume manufacturing.