The Effects of Increasing the Aspect Ratio of GaAs Backside Vias

Holly Rubin, Dwarakanath Geerpuram, Russ Westerman
Plasma-Therm LLC, 10050 16th Street North, Saint Petersburg, FL 33716, USA
Email: holly.rubin@plasmatherm.com, Telephone: (727) 577-4999

Mark Buliszak, Rajesh Baskaran, Allen W. Hanson
M/A-COM Technology Solutions, Inc, 100 Chelmsford Street, Lowell, MA 01851, USA
Email: allen.hanson@macomtech.com, Telephone: (978) 656-2538

GaAs is widely used throughout the wireless telecommunications industry in the manufacture of devices such as high electron mobility transistors (HEMTs). While this material system has excellent electrical properties that lends it well to applications requiring high-efficiency and/or high-frequency operation, this intrinsic performance advantage also requires maintaining low extrinsic parasitics such as ground inductance. A common strategy employed throughout the industry for reducing the effect of this parasitic is the use of through-substrate vias also commonly referred to as backside vias. For frequencies of operation at X-band and above it is common practice to employ transistor designs featuring source contacts that are individually connected to through substrate vias. These vias, often referred to as slot vias[1], can result in very low overall circuit inductance by reducing the lead inductance component of this parasitic, but the approach requires vias of exceedingly small lateral dimension and high aspect ratio. Such reduced dimension vias are also proving enabling to further die shrink for more cost sensitive applications. Consequently, the trend in the industry has been toward higher via densities and shrinking via dimension. While traditional vias have relatively modest aspect ratios (typically 1.7 – 2.5:1), emerging slot via designs are approaching aspect ratios approaching 10:1. Although reducing via geometry may offer these significant advantages, it also presents a unique set of process challenges to photoresist patterning, etch throughput and quality, as well as reliably metalizing these vias. In this paper, we present the results of process development work targeted to address these emerging geometries.

In papers previously presented in this conference we reported a pillar free GaAs via etch process with etch rates greater than 10µm/min for vias with very low aspect ratios of less than one[2,3]. This paper will report etch rates for high aspect ratio slot vias. For aspect ratios as high as 10, in a 5µm x 10µm square slot via etched to a 50µm depth, we are reporting etch rates of 3 um/min. This is a vertical via, with smooth sidewalls, shown in Figure 1.

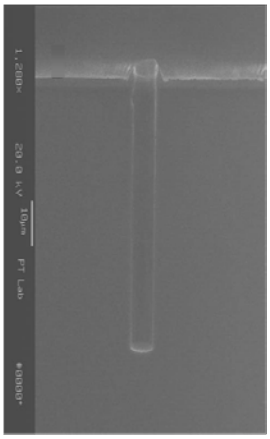

Figure 1: The 5µm side of a 5µm x 10µm slot via etched to a 50µm depth (10:1 AR).

Additional data that will be presented in this paper maps the process space around the high aspect ratio via result shown in Figure 1. The process parameters varied in this study were pressure, total gas flow, and bias power. The responses we analyzed include GaAs etch rate, photoresist etch rate, selectivity, sidewall quality. One of the challenges associated with etching at high GaAs etch rates or at high aspect ratios, is maintaining smooth sidewall quality. We will report in this paper how the selectivity of the GaAs etch rate to the photoresist etch rate correlates to the quality of the sidewall morphology of the vias. We will also present the aspect ratio dependent etch rate data

for both circular and slot vias. This topic has been studied in the past for a RIE only process[4]. This work presents an extension of that curve using an ICP process.

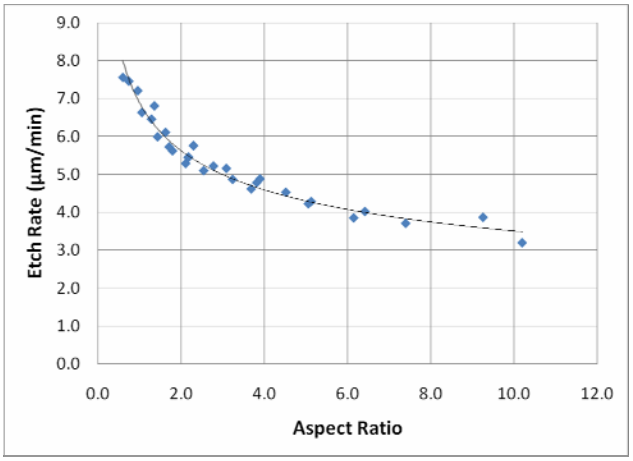

Figure 2: Time averaged etch rate as a function of aspect ratio for slot vias, from 20x25µm to 20x5µm slot vias.

Also presented will be the results of a test reticle created for these studies that features vias of various size and density that was used to quantify etch and plating system interactions. A series of via sizes ranging from 15x5 to 15x30um from the reticle are shown in Fig 3a. This figure exhibits the excellent plating uniformity that was obtained for all via geometries in this series. Fig 3b, and 3c illustrate the extent of plated taper present in the process – metallization thickness was found to consistently maintain approximately 85% of its nominal value from back to front. A similar study involving the effect of via spacing and density and their effect on plasma loading will also be summarized and presented.

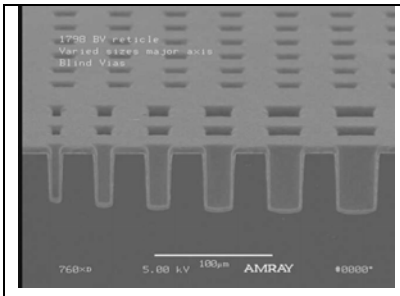

Fig 3a Via sizes:15x10 to 15x35 um

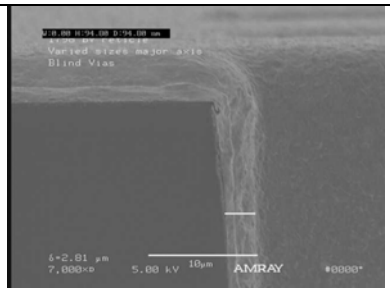

Fig 3b Gold at top sidewall~ 2.8 um

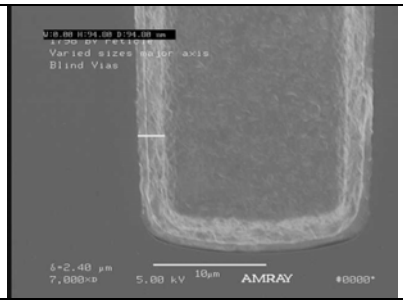

Fig 3c Gold bottom sidewall~ 2.4um

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