

Au-free, High-Breakdown AlGaN/GaN MISHEMTs with Low Leakage, High Yield and Robust TDDDB Characteristics

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Abstract

Extensive characterization was performed on Au-free depletion-mode Metal-Insulator-Semiconductor High Electron Mobility Transistors (MISHEMTs) processed on AlGaN/GaN epitaxial layers on 150 mm Si wafers. MISHEMTs with different gate widths (W_G) up to 100 mm show high yield, hard breakdown voltage beyond 600V and low leakage current at 600V. Good dispersion, low capacitances and excellent time-dependent-dielectric-breakdown (TDDDB) data are also presented.

INTRODUCTION AND MOTIVATION

GaN-based Metal-Insulator-Semiconductor High Electron Mobility Transistors (MISHEMTs) combine high power handling capability with low off-state leakage currents [1-3]. This makes them promising candidates for new generation, high frequency switches for high power converters. A first step towards industrial readiness is to demonstrate good device performance over a large number of samples and across several key parameters and to prove the gate dielectric robustness under high electric field [4,5]. We report on the characterization of 600V Au-free depletion mode AlGaN/GaN MISHEMT power devices with effective gate width up to 100 mm, demonstrating high device yield over 3 wafers. The off-state and maximum current, specific on-resistance, capacitances, dispersion and gate dielectric lifetime are also reported.

DEVICE PROCESSING

The power transistors were fabricated on epitaxial (Al)GaN layers on 150 mm silicon wafers, as shown in figure 1. The gate metal was deposited on a stack formed by 5 nm Al_2O_3 , grown by Atomic Layer Deposition (ALD) on top of 5 nm in-situ Metal-Organic Vapor Deposited (MOCVD) Si_3N_4 [6]. The Al_2O_3/Si_3N_4 film was etched at the drain and source locations, where Ti/Al/W was deposited and alloyed at 600°C to create ohmic contacts. A stack of Ti/Al (20/250 nm) was used for the local interconnections and 10 μ m-thick Cu for the power lines. Plasma Enhanced

Chemical Vapor Deposited (PECVD) SiN layers were used to realize pre-metal and inter-metal dielectrics and for the final passivation.

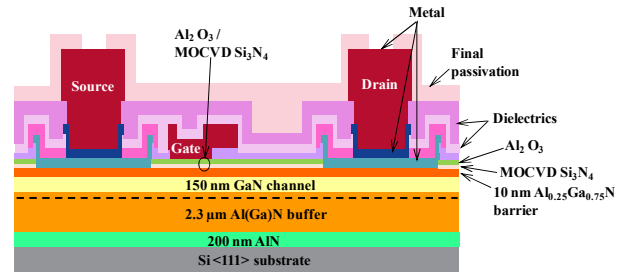


Fig 1. Schematic cross-section of the fabricated MISHEMT.

CHARACTERIZATION AND RESULTS

The yield of multifinger power devices with a total gate width (W_G) ranging from 10 to 100 mm and gate length $L_G=1.5\mu m$ was assessed. Results are reported in figure 2, which shows high yield over 3 wafers.

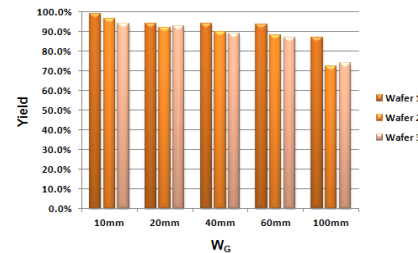


Fig 2. Yield graph, showing the percentage of functioning power transistors with different gate width and on three wafers. On each wafer 345 transistors were measured. Metal shorts, pinch-off behavior and the gate leakage current were tested on each device.

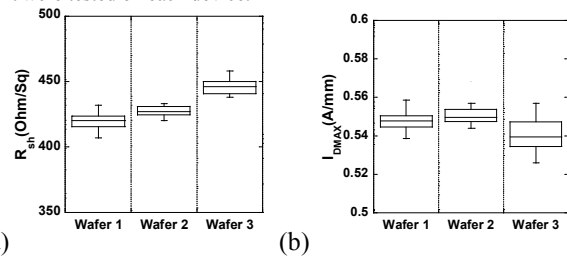


Fig 3. Statistical plots (median, 25% and 75% percentile, max value, min value) of R_{th} (a) and $I_{D_{MAX}}$ of 100 μ m-wide transistors (b).

The uniformity of the process was tested on 3 wafers by measuring the sheet resistance (R_{sh}) of the 2-dimensional electron gas (2DEG) and the maximum drain current $I_{D_{MAX}}$. Figure 3 shows uniform R_{SH} (tested on Van-der-Pauw structures) and $I_{D_{MAX}}$ (measured on 100 μ m-wide transistors at $V_{DS}=10V$ and $V_{GS}=2V$).

The drain off-state leakage current was measured at room temperature on 6 power devices (3 with $W_G=20mm$ and 3 with $W_G=100mm$) by setting V_{GS} at $-7V$ and ramping up V_{DS} until hard breakdown occurred. As illustrated in figure 4, both 20mm- and 100mm-wide devices have hard breakdown voltage $V_{BD}>600V$. Moreover, low leakage current at 600V (i.e. below 100 μ A) is observed.

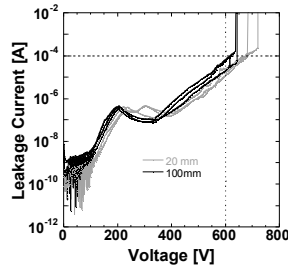


Fig 4. Drain high-voltage leakage current of 20mm- and 100mm-wide transistors with $L_{GD}=9.5 \mu m$ (grey and black lines, respectively).

The maximum drain current $I_{D_{MAX}}$ and specific on-resistance $R_{on,sp}$ were extracted from the output I_D - V_{DS} characteristics. Figure 5 reports the curves of a 20 mm-wide device, which showed $R_{on,sp}=2.9m\Omega \cdot cm^2$ and $I_{D_{MAX}} \approx 8A$.

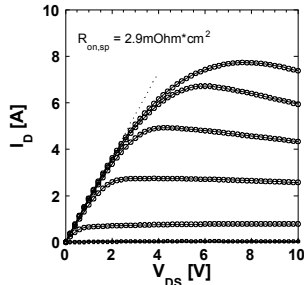


Fig 5. Output curves of a 20 mm-wide transistors with $L_{GD}=9.5 \mu m$.

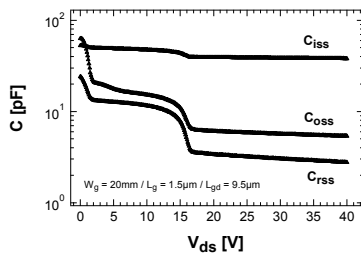
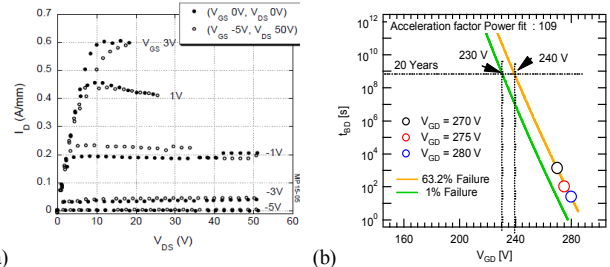


Fig 6. Typical capacitance-voltage curves of three 20mm-wide transistors with $L_{GD}=9.5 \mu m$. $C_{iss} = C_{GS} + C_{GD}$, $C_{oss} = C_{DS} + C_{GD}$, $C_{rss} = C_{GD}$. C_{GS} , C_{DS} and C_{GD} are, respectively, the gate-source, drain source and gate-drain capacitance.

The input, output and reverse transfer capacitances (C_{iss} , C_{oss} and C_{rss} , respectively) of a power transistors with

$W_G=20 mm$ and $L_{GD}=9.5 \mu m$ were measured at 1 MHz for V_{DS} values up to 40V. Results are shown in figure 6, where $C_{iss}=38pF$, $C_{oss}=5.5pF$ and $C_{rss}=2.8pF$ at 40V. As compared with Vertical Double-Diffused Metal-Oxide-Semiconductor (VDMOS) transistors, these values are significantly lower, as expected from GaN HEMTs. Pulsed I-V measurements were performed on devices with $W_G=200 \mu m$ and $L_{GD}=9.5 \mu m$. Figure 7(a) shows low dispersion, measured at $V_{DS}=50V$. Time-dependent-dielectric-breakdown TDDB characterization was performed on 200 μm -wide devices with $L_{GD}=2 \mu m$ (i.e. designed to support an operating voltage up to 60V). This methodology, using a power law extrapolation as shown in figure 7(b), gives a gate dielectric lifetime of 20 years at a gate-to-drain voltage (V_{GD}) of 230 V. We caution against the actual lifetime number, due to the immaturity of reliability prediction in GaN, however emphasize the excellent nature of the gate dielectric.



(a) Pulsed measurements with 400ns pulsewidth. Quiescent bias (V_{GS} , V_{DS})=(0V,0V) (closed symbol) and (V_{GS} , V_{DS})=(-5V,50V) (open symbol). (b) TDDB at room temperature: a time-to-breakdown t_{BD} of 20 years is extrapolated (1% failure) at $V_{GD}=230V$. Devices with $L_{GD}=2 \mu m$ were selected as they allow for testing under much lower voltage levels than the buffer breakdown voltage.

CONCLUSIONS

We report on extensive characterization of Au-free depletion-mode AlGaN/GaN-on-Si MISHEMTs, as a first assessment of technology readiness level. High yield over 3 wafers, low leakage current and high breakdown beyond 600V were demonstrated. Several key parameters were also investigated. Moreover, excellent TDDB results were obtained.

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ACRONYMS

- MISHEMT: Metal-Insulator-Semiconductor High Electron Mobility Transistor
- 2DEG: 2-dimensional electron gas
- ALD: Atomic Layer Deposition
- MOCVD: Metal-Organic Vapor Deposition
- PECVD: Plasma Enhanced Chemical Vapor Deposition
- TDDB: Time-dependent-dielectric-breakdown