40 nm T-Gate Process Development using ZEP Reflow

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Abstract: As III-V compound semiconductor technology extends its reach into the millimeter wavelength (MMW) frequency application space, solid-state power amplifier designs rely heavily on the ability to reduce transistor lateral and vertical dimensions while maintaining high yield. In high-electron-mobility transistors (HEMTs), T-shaped gates are often used to simultaneously attain short gate length and large gate cross-sectional area to reduce electron transit delay time and ensure low gate resistance, respectively. To fabricate sub-0.25 micron T-gates that are necessary for MMW transistor operation, e-beam lithography is often used to define either a bi-layer or tri-layer resist stack for metal liftoff. A common problem that occurs as gate stem length is reduced is known as "metal cathedraling," where metal builds up laterally on the top corners of the bottom resist layer feature and eventually results in a narrow junction between the T-gate stem and head. This undesirable junction can lead to poor electrical contact between the stem and head of the T-gate, and in extreme cases can result in low yield due to detachment/liftoff of the gate head from the stem.

In this presentation, we will discuss the development of a simple technique that helps improve the yield of sub-0.25 micron T-gates by reflow rounding of the bottom ZEP resist feature in a bi-layer ZEP/UV5 stack. This fabrication procedure is outlined in figure 1 below. By using this reflow technique, we have been able to successfully demonstrate 40 nm T-gates with reduced metal cathedraling and improved yield. Process parameters such as ZEP reflow time/temperature, e-beam dose, and the effect of O_2 plasma descum were evaluated during the course of this study. Reflow temperature was found to have the largest effect on reducing ZEP feature size and profile rounding. An optimized process parameter window was determined where ZEP feature size could be controllably reduced by 20 – 40% (depending on initial feature size) as a result of reflow.

The final portion of this talk will discuss experimental results of vertically-scaled AlN/GaN HEMT devices with T-gates fabricated using the reflowed ZEP technique. In devices with T-gate length of 120 nm, we have been able to measure pad de-embedded f_T and f_{max} in excess of 160 GHz with maximum current density of 1.7 A/mm.

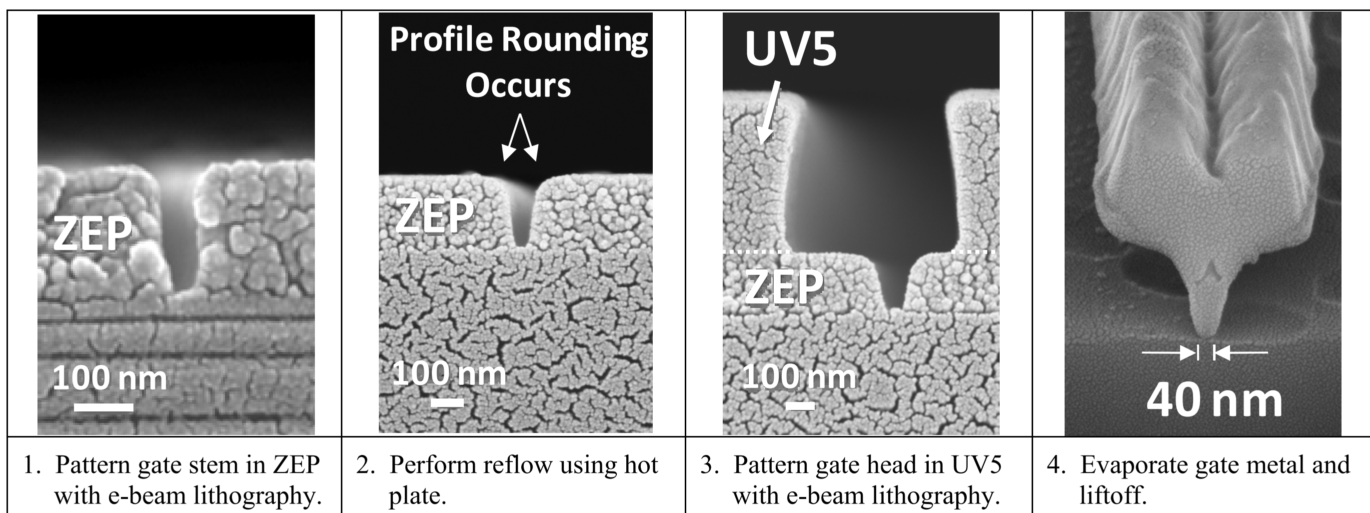

Figure 1: SEM cross-sectional images of the reflowed ZEP T-gate fabrication procedure.