Threshold Voltage Control of Recessed-Gate III-N HFETs Using an Electrode-less Wet Etching Technique

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Recessed-gate structure is one of the common approaches to control the threshold voltage of III-N HFETs. Typically, plasma-enhanced dry etching techniques are used to enable the recessed-gate structures [1,2]. Photo-electrochemical wet etching techniques are also studied [3]. These techniques however often suffer from non-uniform etching that may result in rough etched surface or threshold voltage uniformity issues if the processing is not well controlled [4,5]. In this study, we report a new electrodeless KOH-based wet etching technique and demonstrated the possibility to achieve smooth etched surface and potentially uniform device threshold voltage control in III-N HFETs.

The wet-etching technique was developed using a properly engineered KOH-based aqueous solution was prepared and the etching is facilitated under the illumination of the ultraviolet light without a need for electrodes to catalyze the electrolyte. As shown in Figure 1, an AFM picture shows that the etched area with recessed depth of 30 nm has an RMS surface roughness of 0.37 nm in the gate-recessed region of a AlGaN/GaN HFET, when compared to that of 0.255 nm for the as-grown epi-surface. The smooth etched surface indicates that a uniform etching rate can be achieved with this unique wet etching approach. For comparison, AlGaN/GaN HFETs with and without the recessed gate etching were fabricated and characterized. The measured I_D-V_{GS} curves of a unit-cell HFET (W_G = 300 μm and L_G = 3 μm) are shown in Figure 2. The threshold voltage (V_{th}) is determined at I_{DS} = 1mA/mm in the I_D-V_{GS} transfer curves. V_{th} = -6 V were measured on as-grown HFETs. After the recessed-gate etching, V_{th} is shifted to 0.06 V. The transconductance (g_m) and sub-threshold swing (S) are enhanced to 116 mS/mm and 83 mV/decade, respectively, compared to g_m = 86 mS/mm and S =119 mV/decade for the devices without the recessed gate etching. Figure 3 shows a histogram of the threshold voltage distribution for the recessed gate HFETs. The data points were evaluated from 14 HFETs with different gate widths across a sample size of 1 × 0.5 cm^2. The averaged V_{th} is 0.09 V and the standard deviation for V_{th} is 65 mV. The tight control of V_{th} may suggest that uniform recess depth etching was achieved with the electrode-less wet etching for III-N HFETs. The measured I_D-V_{DS} family curves for as-grown and recessed-gate HFETs, respectively, are also shown for comparison in Figure 4. Although higher on-state resistance is observed due to the higher access resistance in the recessed gate region, the recessed-gate III-N HFETs achieved a $I_{D,max}$ > 400 mA/mm at V_{GS} = 4 V before the gate turns on.

In summary, we report an effective approach to fabricate recessed-gate III-N HFETs using electrodeless KOH-based wet etching technique. Smooth etched surface and potentially uniform device threshold voltage control can be achieved. The results suggest great potential of electrodeless wet etching in achieving large-scale manufacturable III-N transistor fabrication with tight control of threshold voltage for E/D-mode integrated circuits. More details on this technique will be discussed in the conference.

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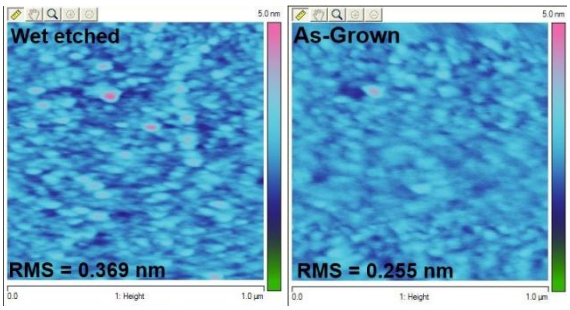

Figure 1. The surface morphology of the recessing etched surface (left) and the as-grown surface (right) measured by AFM.

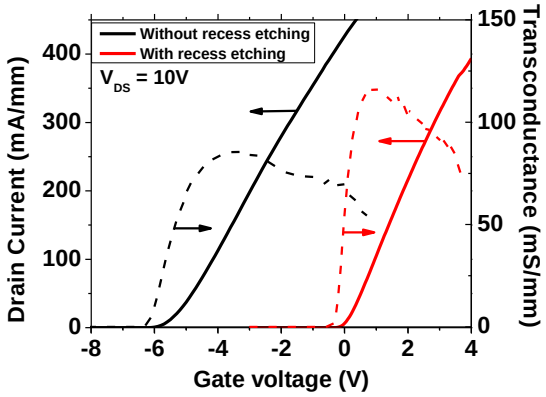

Figure 2. The measured I_D-V_{GS} curves of HFETs with and without gate-recessed etching. The gate length of the device under study is 3 μm.

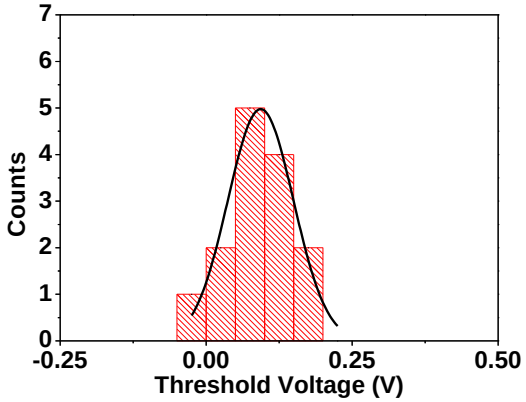

Figure 3. The histogram of measured threshold voltages of HFETs and the fitting of Gaussian distribution with mean of 0.09 V and standard deviation of 56 mV.

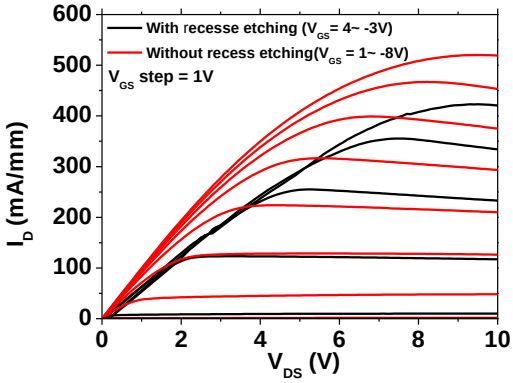

Figure 4. The measured I_D-V_{DS} curves of HFETs with and without the gate-recessed etching. V_{th} for the recessed sample is 0.09 V and that for non-recessed sample is -6 V.

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