

# Evaluation of through wafer via holes in SiC substrates for GaN HEMT technology

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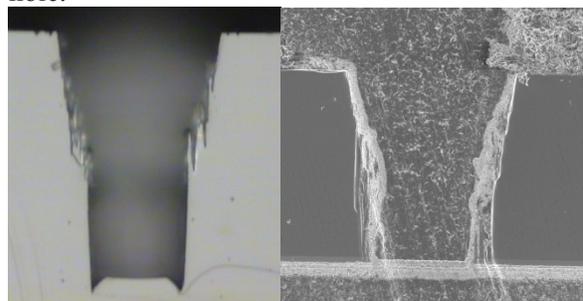
## ABSTRACT

GaN technology arrives at production of IC manufacturers with quite fast evolving processes. Especially backside processes are somehow challenging for GaN technology in concerns of substrate materials used. There exists a lot of experience and know how in backside processing for GaAs and Si substrates. There exists know how for SiC processing but less for the integration of a via hole process in thinned SiC substrates with a active GaN EPI layer in a manufacturing area. In this work there will be presented a evaluation of a SiC via hole process for GaN HEMT technology in terms of quality, integration, reliability and packaging process. The via hole etching process applying a metal hard mask of aluminium structured by lift off or dry chemical etch. These two process variants differ in via hole quality and reliability. Furthermore the pattern – rectangular or circular - of the via will be compared in terms of internal stress of the metal interconnection layer inside the via hole. The SiC ICP etching process evaluation will be shown regarding etch rates and selectivities to the surrounding materials. Remaining residues in the via hole are evaluated and wet chemical treatments characterized for removing the via side wall residuals. The residues analysed by XPS physical analysis explaining the root cause of the generation during via hole etch. Reliability tests and packacking of the different process variants are done revealing the impact of the residues and via pattern. The ion energy of the plasma process has to be very high in order to crack the Si –

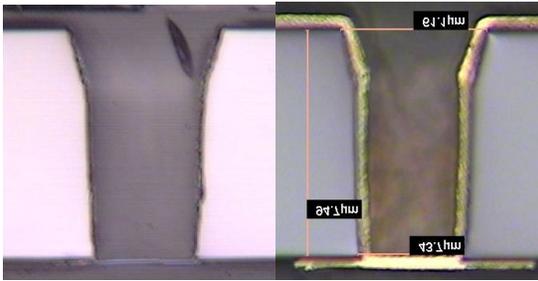
C bonds. That means the process has to be mainly physical assisted. At the plasma etching there is a very high energy necessary to break these bonds. This high energy leads to high temperature dissipation during the via hole process which lead to re deposition processes of the aluminium and built up of Al with chemical bonds to fluorine, the etch gasses used.

The mask has to withstand the high temperature, ion energy and oxygene content of the plasma which means there is a hard mask necessary. As for the SiC etch fluorine chemistry is used there is no way to use a dielectric like silicone oxides or nitrides. That means a metal or a metal compound hard mask has to be used.

The following pictures show the cross section view of a ICP etched hole applying a lift off aluminium mask and a dry etched mask. The roughness of the mask edge in case of lift off process lead to spikes and voids behind the metal in the via hole.

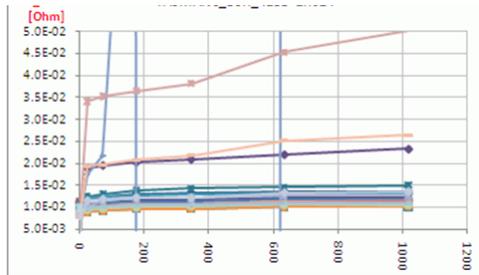


Via blind hole etched by ICP plasma process – Al mask by lift off

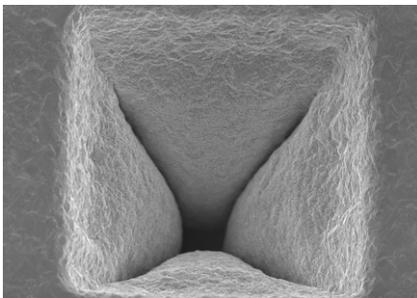


Via blind hole processed by ICP etching - Al etched mask

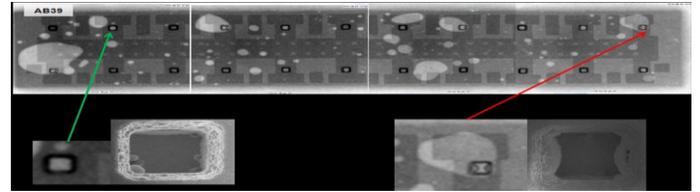
The wet chemical treatment after the SiC etching removes the hard mask. If the residues in the via hole will be not removed it has a great impact on the reliability of the interconnect as shown in the temperature storage data and the x-ray analysis after the soldering process.



R\_via contact resistance during temperature storage test



Top view of failed via hole after temperature storage test – metal de lamination inside the via.



x-ray analysis of soldered die show de lamination effects of metal inside the via

The paper will present the work how to come over of the residues and showing the process approach for high quality and reliable via holes in SiC for GaN HEMT.