III-V MOSFETs for Sub-15 nm Technology Generation CMOS: Some Observations, Issues and Solutions

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High mobility channel materials based on III-V semiconductors are attracting significant attention as a route to enabling continued scaling of CMOS at, and beyond the 15 nm technology generation of the International Technology Roadmap for Semiconductors (ITRS) [1]. To give some insight into the challenges faced in delivering a credible III-V MOSFET technology solution, a number of key factors have to be taken into consideration

i) the mainstream semiconductor industry is now driven by power constrained density scaling, and so gate pitch reduction will continue relentlessly. This places significant challenges at a time when the source/drain contact sizes continue to shrink significantly below lengthscales comparable with the transfer length in conventional III-V ohmic contact schemes. Techniques to realize source-drain contacts with specific contact resistivity below $5x10^{-9}$ Ωcm^2 which can be realized using silicon manufacturing techniques will be required [2].

ii) with the move by Intel to FinFET architectures for the 22 nm CMOS technology generation[3], and an inevitability that other manufacturers will follow suit, any credible sub-15 nm technology generation III-V MOSFET will most likely be non-planar. This means that a device quality gate dielectric must be formed after fin formation, in other words, after the top of the fin has been thru a masking step and the sidewalls have been subjected to a dry etch. Therefore, the use of a "pristine" semiconductor/dielectric interface is likely to be an unaffordable luxury in the final solution.

This presentation will review the current status of both source/drain and gate module development in Glasgow and elsewhere for III-V MOSFETs when mapped against key device performance metrics taken from the ITRS – as summarized in Table 1. Specifically, in the area of source-drain contacts, the formation of silicon compatible, thermodynamically stable, low resistance crystalline metallic phases in high indium concentration $In_xGa_{1-x}As$ layers will be described [4]. For the gate stack, the use of sulphidation techniques prior to dielectric deposition, and subsequent forming gas and post metal anneal strategies strongly mitigate any degradations due to air exposure of the $In_xGa_{1-x}As$ surface [5,6] permitting high channel mobility to be retained and with encouraging on-state and off-state device performance.

References:
[1]www.itrs.net/Links/2009ITRS/Home2009.htm
[2] I.G. Thayne et al., *Microelectron. Eng.* 88 (7), pp1070-1075, 2011
[3] http://newsroom.intel.com/docs/DOC-2032
[4] R. Oxland et al, Submitted to *IEEE Electron Dev. Lett,* Nov 2011
[5] É O'Connor et al., *Appl. Phys. Lett* (accepted)
[6] I.G. Thayne et al., *Proc. SISC,* Dec 2011

Year	2011	2015	2018	2019	2020	2024
Gate Pitch (nm)	76	42	30	27	24	15
Physical Lg (nm)	24	17	13	12	11	7
Source and Drain contact length (nm)	26	13	9	8	7	4
Total Source Drain Resistance ($\Omega\mu m$)	160	140	130	120	120	110
Supply Voltage (V)	0.93	0.81	0.73	0.71	0.68	0.6
Threshold Voltage (V)	0.29	0.21	0.21	0.21	0.22	0.23
Gate Voltage Swing (V)	0.54	0.50	0.41	0.39	0.35	0.25
Saturation Drain Current ($\mu A/\mu m$)	1812	3003	2720	2600	2733	2812
Gate Capacitance ($fF/\mu m$)	0.67	0.5	0.42	0.39	0.37	0.28
Channel Sheet Carrier Density (cm^{-2})	8.5E+12	7.3E+12	7.1E+12	7.2E+12	6.4E+12	5.1E+12
Effective Carrier Velocity (ms^{-1})	1.3E+05	2.6E+05	2.4E+05	2.3E+05	2.6E+05	3.5E+05

Table 1 - Various ITRS metrics and derived parameters taken from the 2009/2010 ITRS Roadmap [1]