Germanium and compound semiconductor manufacturing for advanced CMOS

A. Dimoulas,

MBE Laboratory, NCSR DEMOKRITOS, Athens Greece

The world is rapidly moving into the mobile information age [1] were mobile internet devices (MID) like tablets and smartphones are at the center of attention for consumers, integrated device manufacturers and technology developers. For MIDs and other multimedia applications, control of power consumption at an acceptable level without losing speed is an important requirement. To fulfill this requirement, transistors are made to operate at low power supply voltage, which however leads to performance degradation. Performance boosters such as strained silicon have been extensively used until now, but they are already out of steam so that new solutions are urgently needed. Germanium and III-V compound semiconductors come at a rescue, offering high carrier mobility for the replacement of silicon in the transistor channel to manufacture the next generation advanced CMOS. At present, there is no clear material winner, however a dual channel solution is favored in which p FETs comprise Ge (SiGe) channel while n FETs require InGaAs channel materials [1].

The main technological challenge is the co-integration of the dissimilar channel materials on the same large area (300 mm or larger) Si substrate in a scalable and manufacturable process which will ensure volume production. There are two main routes for co-integration: (a) direct growth on bulk Si via a selective heteroepitaxial growth, (b) semiconductor-on-insulator approach. The obvious advantage of the first approach is its compatibility with Si CMOS manufacturing, low cost and IP re-use. On the other hand, the second approach offers better electrostatic control of the channel, an important requirement to maintain performance in aggressively scaled devices. The focus here will be on the first approach. After a brief review of the problems such as antiphase domains, misfit and threading dislocations and thermal stress which are associated with heteroepitaxial growth of III-Vs on Si, we will shift our attention to possible solutions, focusing on the so called Aspect Ratio Trapping (ART) technology [2]. The latter takes advantage of the well known “necking” effect during growth on patterned substrates where threading dislocations and other defects are confined at the bottom of deep and narrow trenches leaving the top part defect free for device definition. As technology progresses to smaller dimensions, ART becomes more effective and more important. The fabrication of ART-engineered substrates starts with standard STI Si wafers followed by etching to define the narrow trenches. A key enabler is the selective epitaxy of Ge and III-V semiconductors to fill the trenches and produce high quality channel layers. The development of suitable tools is essential to minimize cross contamination and ensure compatibility with Si CMOS processing on large area (300 mm) wafers.

A second important challenge is to develop suitable surface passivation methodologies and gate dielectrics which should be preferably common for both Ge (SiGe) pFET and InGaAs nFET to minimize manufacturing complexity [3]. The research for gate dielectrics for Ge MOS devices has matured although a suitable gate dielectric has not been selected yet. The consensus is that a good quality GeO_2 is essential at least as a thin interfacial layer followed by a metal oxide cap layer. The situation is less clear for InGaAs MOS devices, since the MOS capacitor device characteristics are far from ideal in most cases, for reasons which are not fully understood. Nevertheless, satisfactory MOSFETs with relaxed equivalent oxide thickness (EOT) have been demonstrated indicating that gate dielectrics do not present a fundamental problem which can be solved. The biggest challenge at present is to scale the dielectric to low EOT values (1 nm or lower) as required, without jeopardizing the interface quality between the dielectric and the semiconductor. We will review the state of the art and we will present the most promising gate

dielectric candidates and fabrication methodologies for both type FETs, with an emphasis on scaling to (sub)-1 nm EOT values.

A third important challenge is to develop ohmic contacts for the source and drain regions for both types of FETs in a self-aligned way which will ensure the scaling of these devices in a Si CMOS compatible flow to gate lengths lower than 20 nm as required for the future technology nodes [4]. There is significant progress in self-aligned silicided metal contacts for Ge(SiGe) pFETs and state of the art short channel (20 nm) transistors with excellent performance has been demonstrated. However, it is unclear at present whether a self-aligned "silicide-like" technology for the InGaAs nFETs can be implemented. We will first briefly review the progress in pFET source and drain contacts and we will then emphasize on the most prospective solutions for the nFETs.

In summary, the present work presents a review of the progress in all parts of high mobility (Ge and III-V) advanced CMOS, from the engineered substrates and co-integration schemes, to the channel device structure the gate dielectric and the source and drain contacts. The aim is to identify the main challenges and the prospective solutions which will allow the manufacturing in a Si-compatible flow for volume production.

References

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