

# The DARPA Diverse Accessible Heterogeneous Integration (DAHI) Program: Towards a Next-Generation Technology Platform for High-Performance Microsystems

Sanjay Raman<sup>1</sup>, Carl L. Dohrman<sup>2</sup>, Tsu-Hsi Chang<sup>2</sup>, J. Scott Rodgers<sup>1</sup>

<sup>1</sup>Defense Advanced Research Projects Agency, 3701 N. Fairfax Drive, Arlington, VA 22203, USA

<sup>2</sup>Booz Allen Hamilton Inc., 3811 N. Fairfax Drive, Arlington, VA 22203, USA

Corresponding author contact information: [sanjay.raman@darpa.mil](mailto:sanjay.raman@darpa.mil), +1-571-218-4339

**Keywords:** Compound semiconductor, electronic-photonic integrated circuit, heterogeneous integration, mixed signal circuit, multi-project wafer, foundry, Si CMOS

## Abstract

The development of compound semiconductor (CS) electronics has been motivated by their many superior materials properties relative to silicon. For example, high electron mobility and peak velocity of InP-based material systems have resulted in transistors with  $f_{\max}$  above 1THz [1] as well as ultra-high-speed mixed-signal circuits (see, for example, [2]). The wide energy bandgap of GaN has enabled large voltage swings as well as high breakdown voltage RF power devices [3]. Excellent thermal conductivity of SiC also makes tens of kilowatt-level power switches possible [4]. Meanwhile, in the photonics domain, III-V materials based on InP and GaAs have been a key enabler due to the excellent photonic properties associated with the direct band gap of these materials. The indirect band gap of silicon makes optical gain in this material very inefficient, greatly limiting its utility in both discrete and integrated photonic systems.

On the other hand, silicon CMOS-based technologies have achieved tremendous levels of complexity and integration, while also demonstrating high levels of yield and manufacturability. At the same time, RF CMOS [5] and SiGe HBT [5] device speeds have continued to increase into the multi-100 GHz regime, albeit at the expense of breakdown voltage. These facts can be attributed to the aggressive device scaling and the advanced levels of back-end-of-the-line integration driven by Moore's Law over the past 50 years. In addition, Si-based digital correction and linearization techniques (for example, **Error! Reference source not found.**) have become critical to achieve excellent RF and mixed-signal circuit performance despite drawbacks of the material system. Given these trends, it is our view that the future of III-V electronics depends not on displacing Si, but rather on heterogeneous integration of compound semiconductors with silicon technology in a way that will allow the advantages of the two technology types to be optimally combined.

Heterogeneous integration of compound semiconductors with silicon has been explored in past decades [8][9], but its main practical implementation today is through the use of multi-chip modules or similar assembly techniques. Multi-chip module techniques have been prevalent in various microwave/millimeter-wave RF systems, but performance for high-speed/bandwidth mixed-signal systems has been limited by I/O parasitic effects between chips in such modules and by device and interconnect variability issues. Many of the limitations (including I/O parasitics and phase mismatch) of multi-chip module approaches to heterogeneous integration are governed by the length of separation between CS and Si CMOS devices, and as such, the reduction of this separation is expected to yield dramatic improvements in performance of heterogeneous integrated circuits.

To that end, the U.S. Defense Advanced Research Projects Agency (DARPA) Diverse Accessible Heterogeneous Integration (DAHI) program is developing transistor-scale heterogeneous integration processes to intimately combine advanced compound semiconductor (CS) devices, as well as other emerging materials and devices, with high-density silicon CMOS technology. The ultimate goal of DAHI is to establish a manufacturable, accessible foundry technology for the monolithic heterogeneous co-integration of diverse (e.g., electronic, photonic, MEMS) devices, and complex silicon-enabled architectures, on a common substrate platform for defense and commercial users. The DAHI transistor-level heterogeneous integration approach must overcome a number of difficult technical challenges associated with integration process technology (accurate device-level placement, robust heterogeneous interfaces, dense heterogeneous interconnects, thermal management), manufacturing (transfer of integration technology to state-of-the-art foundries, heterogeneous process yield enhancement, process design kit development, compatibility with computer-aided design tools), and design innovation (innovative circuit design methodologies and architectures

for heterogeneous circuits). If this vision can be achieved with high yield and at reasonable cost, this revolutionary technology will allow circuits in which the optimum device is chosen for each specific function within integrated microsystems encompassing RF/mixed signal, photonics, and MEMS technology. This capability will not only have significant impacts on the performance of both military and commercial microsystems, but it also represents a new paradigm for the CS electronics and photonics communities.

The DAHI program is composed of several thrusts which are developing the integration technologies, design innovations, and manufacturing technologies and expertise which will be required to realize the DAHI vision. One element of DAHI, the Compound Semiconductor Materials on Silicon (COSMOS) program, has demonstrated three different approaches to achieving InP BiCMOS integrated circuit technology featuring InP HBTs and deep submicron Si CMOS [10][11][12]. COSMOS performers are currently pursuing complex heterogeneously integrated mixed-signal circuit designs, including digital-to-analog converters (DACs) with unprecedented SFDR performance in the GHz output frequency regime. DARPA is also pursuing the integration of GaN transistors with Si CMOS on a Si substrate, and DAHI performers have recently demonstrated a monolithically integrated RF amplifier circuit using heterogeneously interconnected GaN HEMTs and pMOS gate bias control [13].

DAHI has also begun transferring COSMOS heterogeneous integration technology to a foundry manufacturing model. In the COSMOS multi-project wafer (MPW) thrust, InP BiCMOS technology is being utilized by a number of expert circuit design teams. The design teams have developed several innovative circuit designs which are expected to demonstrate the utility of heterogeneous integration for microwave communications, imaging, and remote sensing. The COSMOS MPW foundry team is using these multi-project wafer fabrication runs to systematically improve process control and yield while also refining the process design kit used by designers.

Meanwhile, the Electronic-Photonic Heterogeneous Integration (E-PHI) thrust was recently initiated as an element of DAHI. The goal of E-PHI is to enable novel chip-scale electronic-photonics/mixed-signal integrated circuits on a common silicon substrate which offer a considerable performance improvement and size reduction versus current, state-of-the-art technologies. This technology is expected to enable a wide range of novel chip-scale optoelectronic microsystems, including coherent optical systems for sensing (LADAR) and communications, optical arbitrary waveform generators, and multi-wavelength imagers with integrated image processing and readout circuitry. E-PHI will develop process and device technologies for heterogeneous integration as well as novel

architectures for heterogeneously integrated electronic-photonics integrated systems.

In the future, it is anticipated that this expanded portfolio of heterogeneous integration technology modules will be available to designers through a high-yield, manufacturable DAHI foundry technology.

#### REFERENCES

- [1] R. Lai, et al, "Fabrication of InP HEMT Devices with Extremely High Fmax", presented at the 2008 International Conference on Indium Phosphide and Related Materials, Versailles, France.
- [2] S.E. Turner and D.E. Kotecki, "Direct Digital Synthesizer With Sine-Weighted DAC at 32-GHz Clock Frequency in InP DHBT Technology," *IEEE Journal of Solid-State Circuits*, Vol. 41, No. 10, Oct. 2006, pp. 2284-2290.
- [3] Y.F. Wu; M. Moore, A. Saxler, T. Wisler, P. Parikh, "40W/mm Double Field Plated GaN HEMTs," *64th Device Research Conference*, 2006, pp. 151-152.
- [4] Cree's Silicon Carbide Schottky Diode Chip CPW2-1200-S050B.
- [5] C.-H. Jan, et al, "A 45nm Low Power System-On-Chip Technology with Dual Gate (Logic and I/O) High-k/Metal Gate Strained Silicon Transistors," *IEDM Tech. Dig.*, pp. 637-640, 2008.
- [6] Chevalier, P.; et al. "Towards THz SiGe HBTs," *2011 IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM)*, pp.57-65, 2011.
- [7] Adrian Tang, et al. , "A Low Overhead Self-Healing Embedded System for Ensuring High Performance Yield and Long- Term Sustainability of a 60GHz 4Gbps Radio-on-a-Chip", *to be presented, 2012 IEEE International Solid-State Circuits Conference (ISSCC)*, Feb 2012.
- [8] E. L. Friedrich, M. G. Oberg, B. Broberg, S. Nilsson, and S. Valette, "Hybrid integration of Semiconductor Lasers with Si-based single-mode ridge waveguides," *J. Lightwave Technol.* 10, 336-340 (1992).
- [9] M. C. Hargis, R. E. Carnahan, J. S. Brown, and N. M. Jokerst, "Epitaxial lift-off GaAs/AlGaAs metal-semiconductor-metal photodetectors with back passivation", *IEEE Photonics Technology Letters*, vol. 5, no. 10, 1993.
- [10] Augusto Gutierrez-Aitken, , et al., "Advanced heterogeneous integration of InP HBT and CMOS Si technologies for high performance mixed signal applications," *IEEE Microwave Symposium Tech. Dig.*, pp. 1109-1112, 2009.
- [11] T.E. Kazior, et al., "A high performance differential amplifier through the direct monolithic integration of InP HBTs and Si CMOS on silicon substrates," *IEEE Microwave Symposium Tech. Dig.*, pp. 1113-1116, 2009.
- [12] J.C. Li, et al., "Heterogeneous wafer-scale integration of 250nm, 300GHz InP DHBTs with a 130nm RF-CMOS technology," *IEDM Tech. Dig.*, pp. 944-946, 2008.
- [13] T. E. Kazior, et al. "High Performance Mixed Signal and RF Circuits Enabled by the Direct Monolithic Heterogeneous Integration of GaN HEMTs and Si CMOS on a Silicon Substrate", *IEEE Compound Semiconductor IC Symposium (CSICS) Technical Digest*, pp. E1.1-4, 2011.