

# High Breakdown Voltage (1590 V) AlGaIn/GaN-on-Si HFETs with Optimized Dual Field Plates

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## Abstract

In case the peak electric fields at the gate and field plate edges are sufficiently suppressed in field plated AlGaIn/GaN HFETs, the electric field at the drain side first reaches the critical level inducing the channel breakdown. Therefore, the breakdown voltage can be further enhanced by adding a drain field plate that spreads out the potential distribution near the drain side. We have demonstrated state-of-the-art characteristics of AlGaIn/GaN-on-Si HFETs with optimized dual field plates. The breakdown voltage of 1590 V and the specific on-resistance of 1.86 mΩ·cm<sup>2</sup> were achieved for the gate-to-drain distance of 15 μm in which the gate and drain field plate lengths were 2 μm and 1 μm, respectively.

## INTRODUCTION

With the increasing electricity demand and rapid industrial development, the power semiconductor device has become an important part of the power system. It is necessary to keep a high level of power conversion efficiency and output current density for miniaturization of system. As compared with conventional silicon devices, those based on wide bandgap semiconductors such as SiC and GaN offer significantly better performance. In particular, AlGaIn/GaN HFETs are expected to be widely applied in power conversion applications due to their outstanding properties, such as high mobility, high carrier density and high breakdown field strength [1, 2]. Sapphire and SiC were commonly used as substrates because of their lack of large-area GaN bulk crystals. However, recent advancement in growth technology has made it possible to use Si for the substrate, achieving growth of thick epitaxial layers on large-wafer size. Several companies have already commercialized AlGaIn/GaN-on-Si wafers up to a 6-inch diameter [3, 4].

One of the common methods to achieve high breakdown voltages in AlGaIn/GaN HEMTs is to employ a field plate structure [5-7]. In this study, both gate and drain field plates were employed in order to maximize the breakdown voltage for a given channel distance. The effects of the dual field

plates on the breakdown voltage and the specific on-resistance were carefully investigated.

## DEVICE STRUCTURE AND FABRICATION

The schematic cross-sectional view of the AlGaIn/GaN-on-Si HFETs is shown in Fig. 1. The epitaxial structure consisted of a 1.24-nm undoped GaN capping layer, a 20 nm undoped-Al<sub>0.25</sub>Ga<sub>0.75</sub>N barrier, and a 3~4 μm undoped-GaN buffer layer on an N-type Si (111) substrate. The source-to-gate distance, gate length, and gate-to-drain distance were 3 μm, 2 μm, and 15 μm, respectively. The gate field plate length was fixed to be 2 μm whereas the drain field plate length was varied from 1 μm to 8 μm. The gate field plate length was previously optimized for this channel distance.

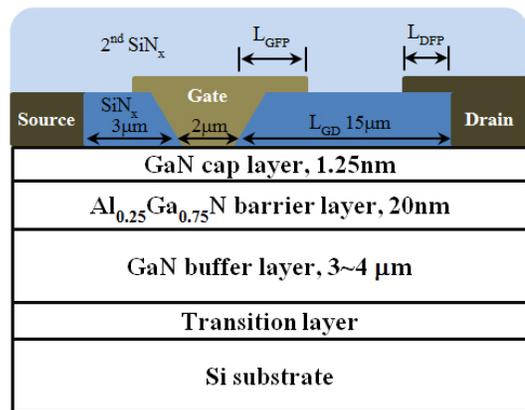


Fig. 1 Schematic cross-sectional view of AlGaIn/GaN-on-Si HFET with dual field plates.

The Mesa-first prepassivation process was employed for device processing [8]. The process sequence is as follows. (1) mesa isolation, (2) SiN<sub>x</sub> passivation film deposition, (3) Ti/Al-based ohmic contact, (4) gate foot patterning and SiN<sub>x</sub> etching, (5) field plate patterning and metallization, and (6) second passivation. A post RTA annealing was carried at 400 °C for 5 min in N<sub>2</sub> ambient to decrease the gate leakage

current, which was attributed to the increase in the barrier height [9].

## RESULTS AND DISCUSSION

The drain field plate length was optimized for the fixed 2  $\mu\text{m}$  gate field plate to effectively spread out the electric field distribution inside the device. It was observed in our simulation study that a single gate field plate was enough to suppress the high electric field at the gate edge and in turn the device breakdown would rather be governed by the locally enhanced electric field at the drain side. The electric field distributions along the 2DEG channel at high drain bias for various drain field plate lengths are compared in Fig. 2. It is suggested that the drain field plate length of 1 - 2  $\mu\text{m}$  is the optimum condition.

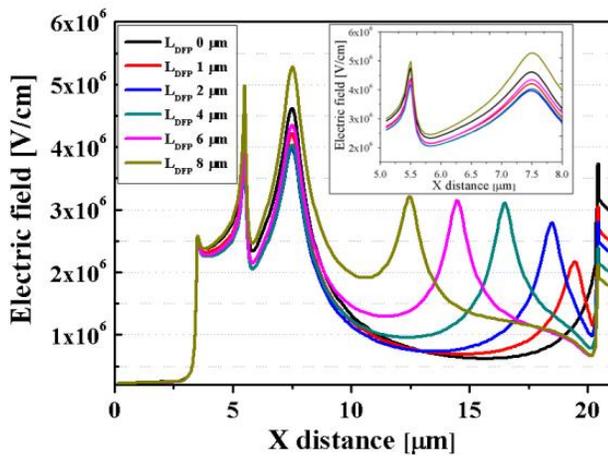
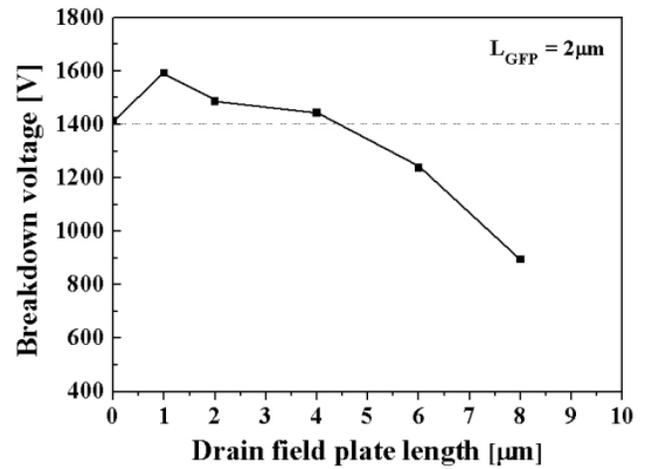
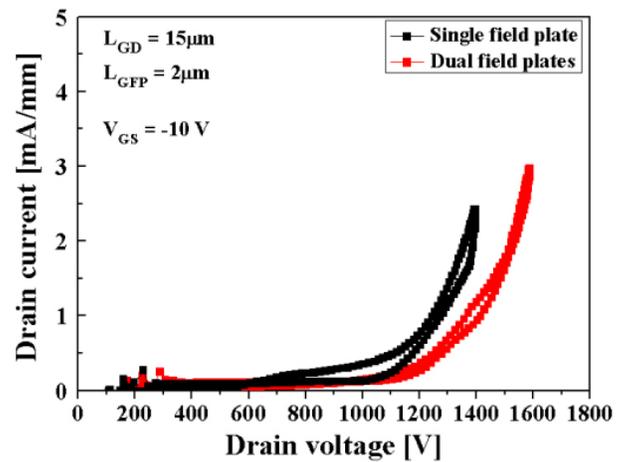


Fig. 2 Electric field distributions along the 2DEG channel at high drain bias for various drain field plate lengths ( $L_{GFP} = 2 \mu\text{m}$ ).

The measured breakdown voltage characteristics of the fabricated devices as a function of drain field plate length are shown in Fig. 3 (a). As expected from the simulation analysis, the breakdown voltage was indeed improved by employing a drain field plate with appropriate lengths. The breakdown voltage of the device fabricated using the optimized dual field plates was enhanced by 12.7% in comparison with the optimized single gate field plate device. The breakdown voltage of 1590 V and the specific on-resistance of  $1.86 \text{ m}\Omega\cdot\text{cm}^2$  were achieved for the gate-to-drain distance of 15  $\mu\text{m}$  in which the gate and drain field plate lengths were 2  $\mu\text{m}$  and 1  $\mu\text{m}$ , respectively. The breakdown characteristics between the optimized single gate field plate device and the optimized dual field plate device are compared in Fig. 3 (b).



(a)



(b)

Fig. 3 (a) Breakdown voltage characteristics of the fabricated dual field plate devices as a function of drain field plate length. The drain field plate length of 0  $\mu\text{m}$  corresponds to the single gate field plate device without the drain field plate. (b) Comparison of the breakdown characteristics between the optimized single gate field plate device and the optimized dual field plate device.

The current-voltage characteristics for various drain field plate lengths are shown in Fig. 4 along with the specific on-resistance values. The specific on-resistance values are almost constant regardless of the drain field plate length. It is because of the positive bias applied on the drain field plate.

The device characteristics achieved in this study are compared with previously reported data in Fig. 5.

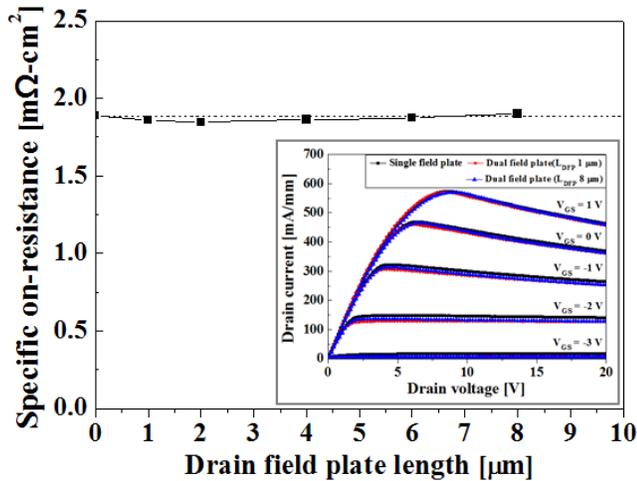


Fig. 4 Specific on-resistance of the fabricated devices as a function of drain field plate length. The inset is the  $I_{DS}$ - $V_{DS}$  characteristics of various dual field plate devices.

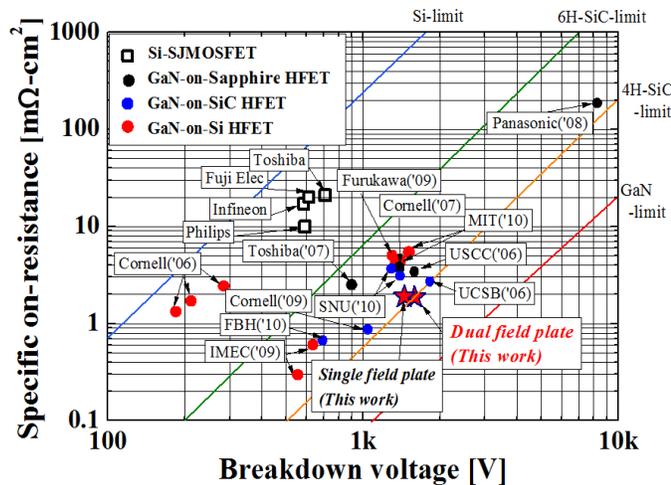


Fig. 5 Performance comparison with previously reported AlGaIn/GaN devices.

## CONCLUSIONS

The dual field plates were successfully employed to maximize the breakdown voltage for a given channel distance in AlGaIn/GaN-on-Si HFETs. For the gate-to-drain distance of 15  $\mu\text{m}$ , the optimum gate and drain field plate lengths were 2  $\mu\text{m}$  and 1  $\mu\text{m}$ , respectively. Though the improvement is not significantly high, it should be noted that no additional process is required to implement the dual field plate structure in comparison with the single gate field plate device.

## ACKNOWLEDGEMENTS

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## REFERENCES

- [1] Y. F. Wu, D. Kapolnek, J. P. Ibbetson, P. Parikh, B. P. Keller, and U. K. Mishra, "Very-High Power Density AlGaIn/GaN HEMTs", IEEE Trans. Electron Devices, Vol. 48, No. 3, pp. 586-590, 2001.
- [2] W. Saito, Y. Takada, M. Kuraguchi, K. Tsuda, I. Omura, T. Ogura, and H. Ohashi, "High Breakdown Voltage AlGaIn-GaN Power-HEMT Design and High Current Density Switching Behavior," IEEE Trans. Electron Devices, Vol. 50, No. 12, pp. 2528-2531, 2004.
- [3] AZZURRO Semiconductors, Power Semiconductor Wafer, <http://www.azzurro-semiconductors.com>.
- [4] NTT AT, GaN Epitaxial Wafer, <http://www.ntt-at.com>.
- [5] H.-Y. Cha, Y.-C. Choi, L. F. Eastman, and M. G. Spencer, "Simulation Study on Breakdown Behavior of Field Plate SiC MESFETs," International Journal of High Speed Electronics and Systems, Vol. 14, No. 3, pp. 884-889, 2004.
- [6] H. Xing, Y. Dora, A. Chini, S. Heikman, S. Keller, and U. K. Mishra, "High breakdown voltage AlGaIn-GaN HEMTs achieved by multiple field plates," IEEE Trans. Electron Devices, Vol. 25, No. 4, pp. 161-163, 2004.
- [7] N. Ikeda, S. Kaya, J. Li, T. Kokawa, M. Masuda, and S. Katoh, "High-power AlGaIn/GaN MIS-HFETs with field-plates on Si substrates," Proc. ISPSD, pp. 251-254, 2009.
- [8] B.-R. Park, J.-G. Lee, H.-J. Lee, J. Lim, K.-S. Seo, and H.-Y. Cha, "Breakdown Enhancement in Field Plated AlGaIn/GaN-on-Si HFETs using Mesa-First Prepassivation Process," Electronics Letters, Vol. 48, No. 3, pp. 181-182, 2012.
- [9] J.-G. Lee, H.-J. Lee, H.-Y. Cha, M. Lee, Y. Ryoo, K.-S. Seo, and J.-K. Mun, "Field Plated AlGaIn/GaN-on-Si HEMTs for High Voltage Switching Applications," J. Korean Phys. Soc. Vol. 59, No. 3, pp. 2297-2300, 2011.

## ACRONYMS

HFET: Heterostructure Field Effect Transistor

$L_{GFP}$ : Gate field plate length

$L_{DFP}$ : Drain field plate length