Manufacturing Efficiency Improvement through MBE Recipe Optimization

Guoliang Zhou and Mark Borek

Skyworks Solutions, Inc., 20 Sylvan Road, Woburn, MA 01801, Tel.781-376-3225, guoliang.zhou@skyworksinc.com

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ABSTRACT

During the MBE growth process of a pHEMT structure, the growth of buffer layer and superlattice generally take more than 70 percent of the overall resources and time. This paper focuses on the reduction of the MBE growth time by optimizing the buffer and superlattice structures, discusses the challenges associated with thinning these layers, and reports results of overall manufacturing efficiency improvement at Skyworks.

INTRODUCTION

Since the initial development of AlGaAs/InGaAs based pHEMT devices 30 years ago, there were numerous publications on refining or optimizing the device structure, but all focused on active device layers to improve the device's electrical performance. To the best of our knowledge, there are few literature reports discussing optimization of the buffer layer and superlattice structure to improve manufacturing efficiency of MBE grown epi wafers. This paper reports the progress of a manufacturing efficiency improvement project at Skyworks, discusses the key aspects that need to be considered when reducing the buffer and superlattice thickness, and reports over 30 percent throughput improvement through MBE growth recipe optimization.

RESULTS AND DISCUSSIONS

A typical pHEMT structure used for today's switch applications consists of active device layers, such as n-GaAs layers, AlGaAs Schottky layers, InGaAs channel layers, and non-active layers such as GaAs buffer layers and superlattices (Fig.1). To grow a high quality pHEMT epi structure, one has to start with a clean crystal surface, which is obtained by thermal desorption of native oxide on the substrate surface. Since thermal desorption of the native oxide process tends to roughen the surface of GaAs substrates, the growth of a buffer layer is necessary to provide a clean and smooth starting surface for the consecutive growth of active device layers. While a thermal-desorption process generally removes most of the surface contamination with the native oxide, it often leaves some residual impurities, such as carbon, silicon, and oxygen. Those impurities can act as acceptors or donors to produce charges near the epitaxial-substrate interface; a buffer layer is also important to separate them from the active device layers. In addition to a GaAs buffer, a GaAs/AlGaAs superlattice in pHEMT structure is mainly used for blocking the hot electrons injection from the InGaAs channel into the buffer to minimize leakage current through the buffer layer. In addition, combining with GaAs buffer, the superlattice also acts as a spacer to separate the channel from the impurities at the epitaxial-substrate interface.

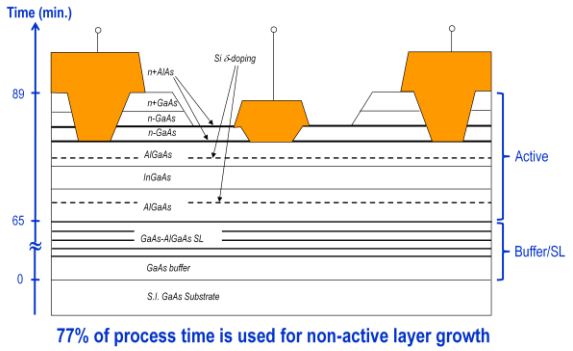

Fig.1. A typical pHEMT structure used in Skyworks products. The axis on the left side marks the growth time required to complete the epi layers.

During the MBE growth cycle of a typical pHEMT structure, only less than 30 percent of the time is spent on the growth of active device layers. The majority of the process time and resources are used for thermal desorption of native oxide, and the growth of the buffer layer and superlattice. While these process steps are essential to obtain high quality pHEMT devices with good electrical performance, it is desirable to minimize those process steps as much as possible in order to maximize production efficiency or throughput, which will ultimately

translate into per wafer cost reduction. The goal for this project is to improve MBE throughput by 30 percent. We took the evolutionary approach by dividing the whole process into several phases in order to minimize production risks. The main focused areas are: the thermal desorption process, the GaAs buffer layer thickness, and superlattices (superlattice periods and the total superlattice thickness). Fig.2 is a schematic that uses x, y, and z axes to represent the above mentioned three areas and illustrates how we can achieve 30 percent reduction of growth time in two steps. Each step achieves about 15 percent improvement.

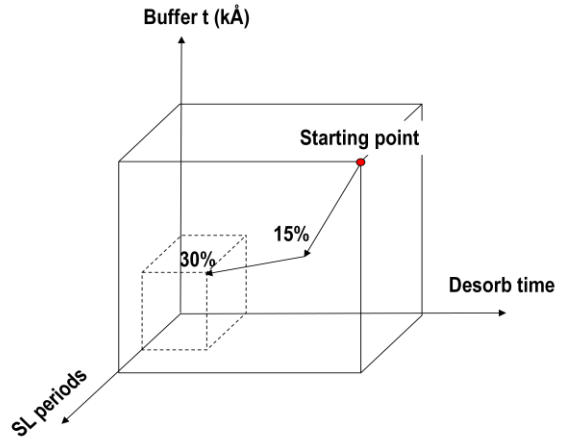

Fig.2. Schematic diagram shows that the process can be optimized in three areas during pHEMT epi process to reduce total growth time by 30%.

For the MBE growth of the GaAs layer, thermal desorption of surface oxide at a high temperature (~600ºC or above) with an overpressure of arsenic is a commonly used method to get an epi ready clean surface. The effectiveness of the thermal desorption process is determined by the cleanness of the epitaxial-buffer interface, which is dependent on both temperature and duration of the thermal desorption process. In general, as long as the temperature is higher than that of oxide desorption threshold, the higher the desorption temperature used, the less desorption time that is required to get a clean surface. On the other hand, the thermal desorption of native oxide process (especially for more stable Ga_2O_3) will roughen the GaAs surface [1-4]. The higher the temperature used, the rougher the surface after oxide removal. A GaAs buffer layer is required to restore a smooth surface for the active device layers. After removal of native oxide, there are usually some residual impurities left on the substrate surfaces. The common impurities are oxygen, carbon, and silicon. The densities of impurities at epitaxial-substrate interface is highly dependent on the thermal desorption process (both temperature and duration). The impact of the residual impurities to device performance will depend on both their densities and the distance between the InGaAs channel and the impurities (epitaxial-substrate interface). Therefore, the optimization of thermal desorption time, the buffer thickness, and the superlattices has to be proceeded dependently in order to minimize the total MBE process time.

During this project, we selected a group of material and device parameters to be closely monitored to ensure that material quality is not sacrificed during our recipe optimization process. Those parameters include surface roughness, sheet charge and mobility, drain saturation current (Idss) and pinch-off voltage (Vp), and leakage current and breakdown voltage. We first focused on minimizing thermal desorption time and GaAs buffer thickness to achieve a 15 percent reduction of the epi process time. Then during the second phase of this project, we focused more on reducing the total thickness of superlattices. To our surprise, we found that surface roughness was not the limiting factor to our buffer thickness reduction effort. Both atomic force microscope (AFM) and KLA-Tencor Surfscan data revealed that surface roughness and average haze level is virtually unchanged even with the GaAs buffer thickness down to 0.1 µm under a typical thermal desorption temperature around 600ºC. However, it became evident that further reduction of buffer thickness was accompanied by the increase of sheet resistance (or decrease of sheet charge and mobility) and charge dispersion when the total combined thickness of buffer and superlattices was less than 0.5 µm (as shown in Fig.3). The fabricated pHEMT devices with very thin buffer and superlattices showed downward shift of drain current (Idss) and positive shift of pinch-off voltage (Vp) distributions. We believe this shift is caused by the positive charge trapped at the substrate/buffer interface. As illustrated by band diagrams in Fig.4, the band adjacent to substrate/epi interface will be lifted up and form a “hump” if there are total net positive charges trapped at the interface region. If the

buffer layer is thick enough (solid line), the "hump" (or the p-region) is relatively far away from the quantum well and sits on the flat portion of the band (see Fig.4). Therefore, it has very little influence to

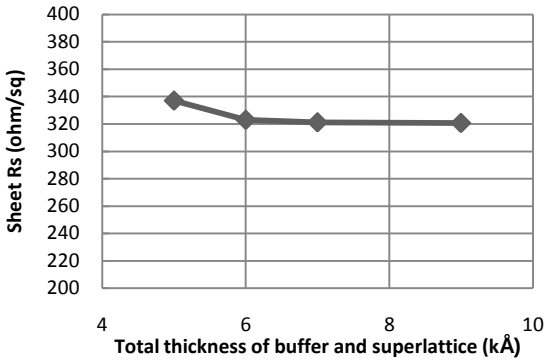

Fig.3. The sheet resistance of pHEMT structures increases when combined total thickness of GaAs buffer layer and AlGaAs-GaAs superlattices is less than 0.5 µm.

the device active region. When the "hump" is moved too close to the quantum well, which is the case when total combined thickness of GaAs buffer layer and AlGaAs/GaAs superlattices becomes too thin, it will lift up the quantum well from Fermi level (as illustrated by the dashed line in Fig.4), thus reducing the sheet charge in InGaAs quantum well and increasing the sheet resistance.

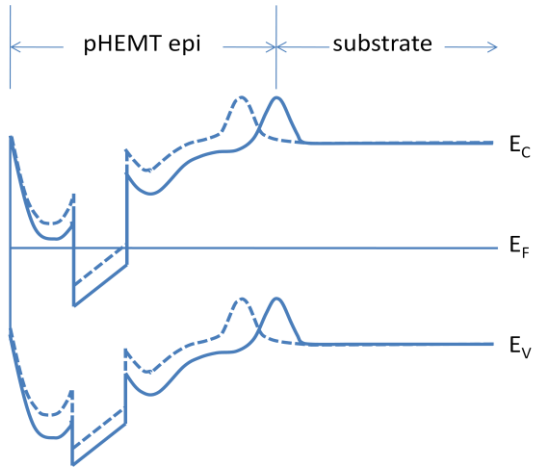

Fig.4. Band diagram illustrates a pHEMT structure with trapped positive charge at epitaxial-substrate interface. The solid (dashed) line represents a pHEMT with thick (thin) buffer. Superlattice structure is not shown in the diagram for simplicity.

As previously mentioned, the most common impurities at the epitaxial-substrate interface are oxygen, carbon, and silicon. Among those impurities, carbon has been reported to act as acceptors providing positive charges at the interface, therefore being responsible for the backgating effect in MBE grown GaAs/AlGaAs HEMTs [5]. We believe that sheet resistance increase with the decrease of buffer thickness is due to the same reason caused by the residual carbon at substrate/buffer interface. The more charges trapped at substrate/buffer interface, the thicker the buffer layer required to screen its influence to the active region. In our case, interface carbon has clearly become the limiting factor for further reducing buffer and superlattice thickness. In order to reduce the density of carbon acceptors accumulated at the epitaxial-substrate interface, a method of "thermal etching" of the substrate at 750ºC in an MBE chamber has been reported [6]. However, "thermal etching" of GaAs substrate in a vacuum at such a high temperature generally will accompany a very rough surface. Therefore, a thick buffer will be required to restore a smooth surface for pHEMT growth, which in turn defeats the purpose of shortening total MBE process time. During this project, we experimented with different process conditions for thermal desorption of native oxide on the GaAs substrate. It was found that carbon density is very sensitive to desorption temperature when the temperature is around ~600ºC or above, while oxygen and silicon densities are more sensitive to desorption time. Fig. 5 shows the SIMS depth profiles of carbon from three pHEMT epi wafers processed under three conditions (standard process, modified process-1, and modified process-2). Both modified process-1 and 2 use slightly elevated desorption temperature (50ºC higher), but modified process-2 also shortened the standard desorption time by half. Table 1 lists the total doses of carbon, oxygen, and silicon at epitaxial-substrate interface under these three process conditions. With a 50ºC increase of temperature, the carbon density has been reduced by four times in both modified processes, regardless of desorption time. In contrast, the lowest oxygen and silicon doses can only be achieved at a higher temperature with standard desorption time. That 50ºC increase of temperature is not enough to offset the 50 percent reduction in process time in order to effectively remove oxygen and silicon.

Through optimizing our thermal desorption process, we have determined an optimal growth condition that allows us to reduce the total thickness

of the GaAs buffer and superlattices and maintain the requirements of minimum interface contamination and surface roughness. Over 30 percent improvement of MBE production throughput has been achieved by optimizing the growth recipe. PHEMT devices processed based on the epi structure with 30 percent of recipe time reduction was fully characterized

	C(10^{12}/cm^2)	O(10^{12}/cm^2)	Si(10^{12}/cm^2)
Std. process	31.9	0.14	0.64
Process-1	7.9	0.02	0.25
Process-2	7.2	3.1	7.2

Table 1, Residual contamination (in doses) of carbon, oxygen, and silicon at epitaxial-substrate interface measured by SIMS depth profiles from three different thermal desorption processes.

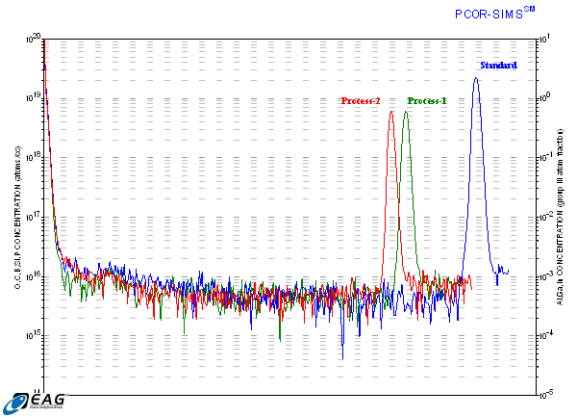

Fig.5. SIMS depth profiles of carbon from three pHEMT epi wafers processed under three different conditions. The carbon doses for both modified processes are 4 times lower than that of standard, but there is virtually no difference between Process-1 and 2.

through all the metrologies and device parametrics, including high temperature operating life (HTOL) test. The device performance data showed no sign of degradation due to shortening the MBE growth time. The modified process has been implemented to most high volume products through different phases. The year-over-year MBE throughput improvement through recipe optimization and other projects at Skyworks is shown in Fig.6.

CONCLUSIONS

During a traditional MBE growth process of pHEMT epi structures, over 70 percent of time was spent on removing native oxide, and growing buffer and superlattices. In order to optimize process efficiency, all three components have to be considered dependently. The main challenge for reducing buffer/supperlace thickness without sacrificing device performance is minimizing carbon concentration at the epitaxial-substrate interface while still maintaining surface smoothness for active epi layers. By modifying the thermal desorption process, a 30 percent reduction of total growth time has been achieved at Skyworks.

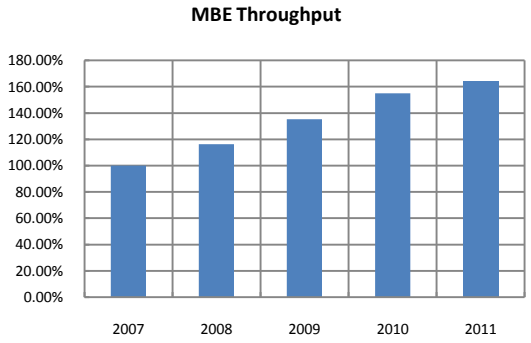

Fig.6. Year over year MBE throughput improvement at Skyworks through recipe optimization and other engineering projects.

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ACRONYMS:

MBE: Molecular Beam Epitaxy
pHEMT: Pseudomorphic High Electron Mobility Transistor
SIMS: Secondary Ion Mass Spectroscopy
AFM: Atomic Force Microscope