A New Single Wafer Cleaning Technology for Compound Semiconductor Manufacturing

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Abstract

We have developed a novel single wafer cleaning technology that targets the needs of compound semiconductor manufacturing: removal of photoresist and post-etch residue while maintaining compatibility with a myriad of compound semiconductor materials, exposed metals, and dielectric layers. The CoatsClean™ platform is a combination of both process and chemical technology featuring significantly reduced chemical usage, short process times, wafer-to-wafer consistency, and process flexibility. In this paper, the CoatsClean™ technology is described and results are shown that demonstrate the capability to remove post-etch residue in the production of GaAs heterojunction bipolar transistors (HBT)s for both polyimide via and base pedestal layers.

INTRODUCTION

We have developed a novel single wafer cleaning technology that targets the needs of compound semiconductor manufacturing: removal of photoresist and post-etch residue while maintaining compatibility with a myriad of compound semiconductor materials, exposed metals, and dielectric layers. The CoatsClean™ platform is a combination of both process and custom chemical formulation technology. The innovation results from the insight that wafer cleaning is a chemical process and the conscious choice to design the optimal chemical process for wafer cleaning. This technology features significantly reduced chemical usage, point-of-use heating, and short process times in a single bowl tool. In addition to environmental sustainability, the reduced chemical usage allows the use of fresh, unused solution on every wafer leading to wafer-to-wafer consistency and a cost of ownership that can be lower than other resist stripping processes used to fabricate GaAs HBTs including plasma-based dry strip, single wafer spray, and immersion.[1-2] This technology provides flexibility in photoresist cleaning processes including the ability to balance resist removal with materials compatibility, increased stability of chemical formulations, and the ability to run multiple wafer types and chemistries on the same tool. In this paper, the CoatsClean™ technology is described, and results are shown that demonstrate the capability to remove post-etch residue in the production of GaAs HBTs.

COATSCLEAN PROCESS DESCRIPTION

The CoatsClean™ process was performed using a newly developed EVG-301RS single-wafer photoresist stripping system designed expressly for the implementation of CoatsClean™ technology. The post-etch residue was removed using an organic solvent based formulated stripper. The CoatsClean™ process is a multi-step process performed in a single bowl, which enables a small tool footprint. Wafers are coated with the formulated stripper with a sufficient volume to coat completely only the wafer's top surface, resulting in significantly reduced chemical usage per wafer compared to immersion or single wafer spray tools. Next, using point-of-use heating, the formulation is heated on the wafer. Point-of-use heating offers flexibility to process different wafer types at different temperatures on the same tool and in the same bowl. After heating, the formulation is initially rinsed with a small volume of fresh formulation followed by spray rinsing with water. Finally, the wafer is dried by spin drying. In addition to reduced chemical usage, the use of fresh, unused solution on every wafer leads to wafer-to-wafer consistency and increased stability of chemical formulations because the chemicals stored in the tool are held at room temperature rather than at elevated cleaning temperatures. Overall, the CoatsClean™ technology provides a new approach to photoresist removal and wafer cleaning that provides environmental sustainability and a lower cost of ownership compared to traditional resist strip processes.

POLYIMIDE VIA RESIST STRIP

CoatsClean™ technology was used to remove post-etch residue for two different etch processes. The first process was the polyimide via etch between Metal-1 and Metal-2. Vias were patterned in a positive photoresist then etched through the polyimide using an O_2 plasma. To strip the remaining photoresist from the underlying polyimide, a single

150 mm wafer was coated with CoatsClean formulation. After 30 sec of exposure to the CoatsClean formulation to dissolve the remaining resist, the wafer was rinsed with fresh formulation followed by a spray rinse with DI water, then dried by spin drying. The total process time for one wafer was less than 2 minutes with a total volume usage of formulation of less than 40 mL per wafer. Figure 1 shows SEM images before and after the CoatsClean™ resist strip process, clearly showing the removal of the resist layer from the underlying polyimide film. Wafers were inspected using a Rudolph NSX-100 automated optical inspection system. A wafer map from the NSX showing die yield for a CoatsClean™-stripped wafer is shown in Figure 2, indicating good stripping performance. Electrical characterization is needed to ensure device performance on wafers processed using CoatsClean™ for the PV strip.

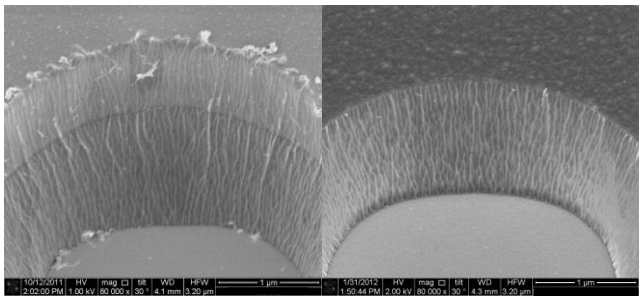

Figure 1. SEM images of the PV strip process: [left] unstripped showing photoresist (top layer) and polyimide (bottom layer), and [right] after the CoatsClean™ strip showing only the polyimide layer.

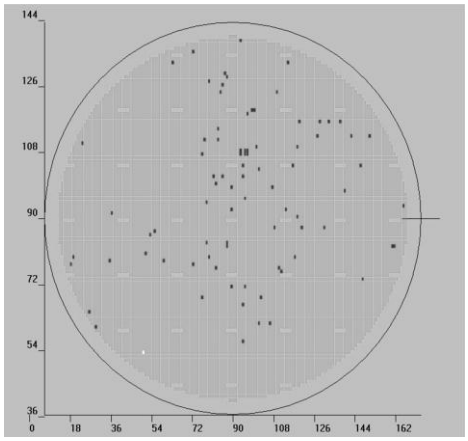

Figure 2. NSX-100 wafer map for the PV strip process with CoatsClean™ showing 99.3% die yield.

BASE PEDESTAL RESIST STRIP

The second process was the plasma etch to form the base pedestal in a GaAs HBT. To strip the post-etch residue from the BP mesa, a single 150 mm wafer was coated with the same CoatsClean™ formulation used for the PV strip. After coating, the formulation was heated for a total of 60 sec. Figure 3 shows a plot of liquid temperature vs. time. In this heating regime, the temperature was dynamic, with a maximum temperature of 125°C at 60 sec. After heating, the wafer was then rinsed with fresh formulation followed by a spray rinse with DI water, then dried by spin drying. The total process time for one wafer was less than 3 minutes with a total volume usage of formulation of less than 35 mL per wafer.

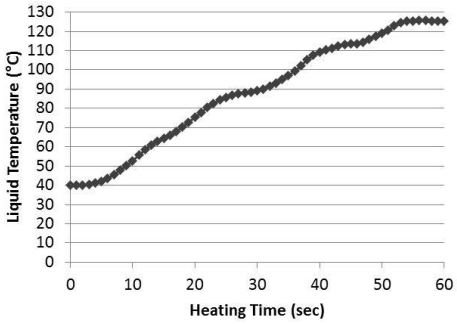

Figure 3. Liquid temperature vs. heating time for the BP strip process. The liquid temperature was measured by immersing a thermocouple bead in solution on a wafer in the EVG 301RS.

Figure 4 shows SEM images before and after the CoatsClean™ strip process, clearly showing the removal of the post-etch residue from the BP mesas. This CoatsClean™ BP strip process was used to strip post-etch residue after the BP etch on four full-flow wafers. These wafers were inspected using a Rudolph NSX-100 automated optical inspection system. Wafers maps from the NSX comparing a CoatsClean™-stripped wafer to a wafer stripped using the standard Skyworks process (solvent-based bath and spray cleaning) are shown in Figure 5, indicating comparable stripping performance. Electrical characterization is needed to ensure device performance on wafers processed using CoatsClean™ for the BP strip.

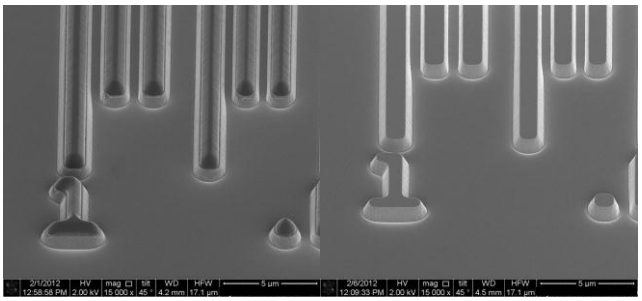

Figure 4. SEM images of the BP strip process: [left] unstripped and [right] after CoatsClean™ strip.

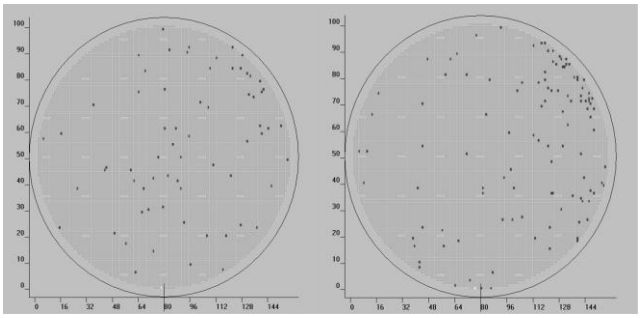

Figure 5. NSX-100 wafer maps for the BP strip on full-flow wafers: [left] CoatsClean™ processed wafer with 99.4% die yield and [right] standard Skyworks processed wafer with 99.1% die yield.

CONCLUSIONS

We have developed a novel single wafer cleaning technology that meets the needs of GaAs HBT manufacturing. The CoatsClean™ technology was used successfully to remove photoresist after a PV etch process and to strip post-etch residue after the BP etch process. Both the PV strip and BP strip processes have short process times and low chemical usage.

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REFERENCES

[1] J. Wang, et al., *Oxygen Plasma Photoresist Strip in High Volume HBT Production*, 2004 CS Mantech Technical Digest.

[2] A. Machamer, "Wet Cleaning" in *Semiconductor Manufacturing Handbook*, H. Geng (ed.), McGraw-Hill, New York (2005), pp. 18.1-18.4.

ACRONYMS

HBT: Heterojunction Bipolar Transistor
BP: Base Pedestal
PV: Polyimide Via
DI: Deionized
SEM: Scanning Electron Microscopy