The DARPA Diverse Accessible Heterogeneous Integration (DAHI) Program: Towards a Next-Generation Technology Platform for High-Performance Microsystems

Sanjay Raman[1], Carl L. Dohrman[2], Tsu-Hsi Chang[2], J. Scott Rodgers[1]

[1]Defense Advanced Research Projects Agency, 3701 N. Fairfax Drive, Arlington, VA 22203, USA
[2]Booz Allen Hamilton Inc., 3811 N. Fairfax Drive, Arlington, VA 22203, USA

Corresponding author contact information: sanjay.raman@darpa.mil, +1-571-218-4339

Keywords: Compound semiconductor, electronic-photonic integrated circuit, heterogeneous integration, mixed signal circuit, multi-project wafer, foundry, Si CMOS

The views, opinions, and/or findings contained in this article/presentation are those of the author/presenter and should not be interpreted as representing the official views or policies, either expressed or implied, of the Defense Advanced Research Projects Agency or the Department of Defense.

Abstract

The DARPA Diverse Accessible Heterogeneous Integration (DAHI) program is developing transistor-scale heterogeneous integration processes to intimately combine advanced compound semiconductor (CS) devices, as well as other emerging materials and devices, with high-density silicon CMOS technology. DAHI is pursuing a holistic approach to heterogeneous integration which includes initiatives in high performance electronics, electronic-photonic integration, and the establishment of a high-yield heterogeneous integration foundry capability. The DAHI program seeks to establish a new paradigm in which microsystems designers will have freedom to utilize a diverse array of materials and device technologies on a common substrate platform.

INTRODUCTION

The development of compound semiconductor (CS) electronics has been motivated by their many superior materials properties relative to silicon. For example, high electron mobility and peak velocity of InP-based material systems have resulted in transistors with f_{max} above 1THz [1] as well as ultra-high-speed mixed-signal circuits (see, for example, [2]). The wide energy bandgap of GaN has enabled large voltage swings as well as high breakdown voltage RF power devices [3]. Excellent thermal conductivity of SiC also makes tens of kilowatt-level power switches possible [4]. Meanwhile, in the photonics domain, III-V materials based on InP and GaAs have been a key enabler due to the excellent photonic properties associated with the direct band gap of these materials. The indirect band gap of silicon makes optical gain in this material very inefficient, greatly limiting its utility in both discrete and integrated photonic systems.

On the other hand, silicon CMOS-based technologies have achieved tremendous levels of complexity and integration, while also demonstrating high levels of yield and manufacturability. At the same time, RF CMOS [5] and SiGe HBT [6] device speeds have continued to increase into the multi-100 GHz regime, albeit at the expense of breakdown voltage. These facts can be attributed to the aggressive device scaling and the advanced levels of back-end-of-the-line integration driven by Moore's Law over the past 50 years. In addition, Si-based digital correction and linearization techniques (for example, [7]) have become critical to achieve excellent RF and mixed-signal circuit performance despite drawbacks of the material system. Given these trends, it is our view that the future of CS electronics depends not on displacing Si, but rather on heterogeneous integration of compound semiconductors with silicon technology in a way that will allow the advantages of the two technology types to be optimally combined.

As an example of the potential benefits of heterogeneous integration, consider the plot of Johnson figure of merit (product of transistor cutoff frequency and breakdown voltage) [8] versus integrated circuit complexity (as measured by transistor count) for several semiconductor material and device types, as shown in Figure 1. Si CMOS is by far the superior material system in terms of integration complexity, exceeding the most advanced CS material (InP) by over five orders of magnitude. However, its Johnson figure of merit is exceeded by several CS materials by an order of magnitude. Nitride-based semiconductors (represented by GaN in Figure 1) possess the highest Johnson figure of merit of currently utilized semiconductor materials; however, nitrides have only rudimentary integration complexity to date. CS materials such as GaN and InP would benefit greatly from leveraging novel silicon-enabled circuit or system architectures to enhance the performance of advanced CS-based RF/mixed signal circuits.

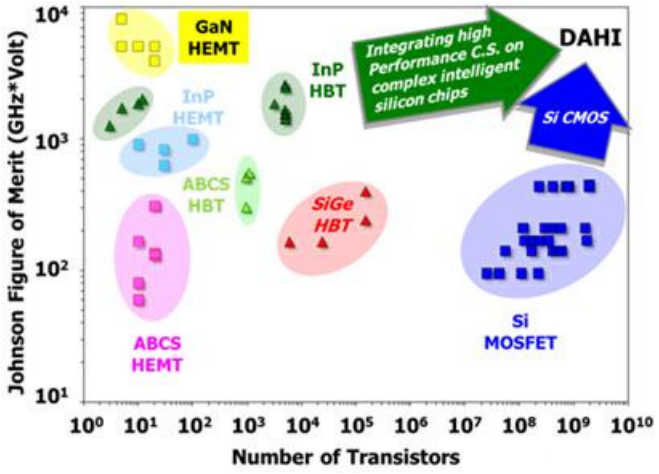

Figure 1: Plot of Johnson Figure of Merit (product of transistor cutoff frequency and breakdown voltage) vs. Integration Complexity (number of transistors per circuit) classified by a variety of material and device technologies.

Heterogeneous integration of compound semiconductors with silicon has been explored in past decades [9][10], but its main practical implementation today is through the use of multi-chip modules or similar assembly techniques. Multi-chip module techniques have been prevalent in various microwave/millimeter-wave RF systems, but performance for high-speed/bandwidth mixed-signal systems has been limited by I/O parasitic effects between chips in such modules and by device and interconnect variability issues. Many of the limitations (including I/O parasitics and phase mismatch) of multi-chip module approaches to heterogeneous integration are governed by the length of separation between CS and Si CMOS devices, and as such, the reduction of this separation is expected to yield dramatic improvements in performance of heterogeneous integrated circuits.

To that end, the U.S. Defense Advanced Research Projects Agency (DARPA) Diverse Accessible Heterogeneous Integration (DAHI) program is developing transistor-scale heterogeneous integration processes to intimately combine advanced compound semiconductor (CS) devices, as well as other emerging materials and devices, with high-density silicon CMOS technology. The ultimate goal of DAHI is to establish a manufacturable, accessible foundry technology for the monolithic heterogeneous co-integration of diverse (e.g., electronic, photonic, MEMS) devices, and complex silicon-enabled architectures, on a common substrate platform for defense and commercial users. The DAHI transistor-level heterogeneous integration approach must overcome a number of difficult technical challenges associated with integration process technology (accurate device-level placement, robust heterogeneous interfaces, dense heterogeneous interconnects, thermal management), manufacturing (transfer of integration technology to state-of-the-art foundries, heterogeneous process yield enhancement, process design kit development, compatibility with computer-aided design tools), and design innovation (innovative circuit design methodologies and architectures for heterogeneous circuits). If this vision can be achieved with high yield and at reasonable cost, this revolutionary technology will allow circuits in which the optimum device is chosen for each specific function within integrated microsystems encompassing RF/mixed signal, photonics, and MEMS technology. This capability will not only have significant impacts on the performance of both military and commercial microsystems, but it also represents a new paradigm for the CS electronics and photonics communities.

PROGRAM DETAILS

The DAHI program is composed of several thrusts which are developing the integration technologies, design innovations, and manufacturing technologies and expertise which will be required to realize the DAHI vision. One element of DAHI, the Compound Semiconductor Materials on Silicon (COSMOS) thrust, has demonstrated three different approaches to achieving InP BiCMOS integrated circuit technology featuring InP HBTs and deep submicron Si CMOS [11][12][13]. COSMOS performers are currently pursuing complex heterogeneously integrated mixed-signal circuit designs, including digital-to-analog converters (DACs) with unprecedented SFDR performance in the GHz output frequency regime. As part of COSMOS, a team led by Northrop Grumman has demonstrated DACs with SFDR an average of 74.5dBc over a 0.75-1.25GHz frequency range [14]. This exceeds the current state-of-the-art DAC SFDR by over 12dB within this frequency range (see Figure 3).

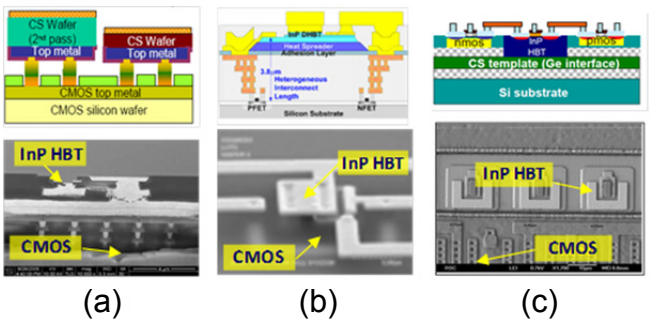

Figure 2: Heterogeneous integration processes being pursued in the COSMOS program, (a) micrometer scale assembly, (b) epitaxial layer printing, and (c) monolithic epitaxial growth using a multi-layered lattice-engineered substrate.

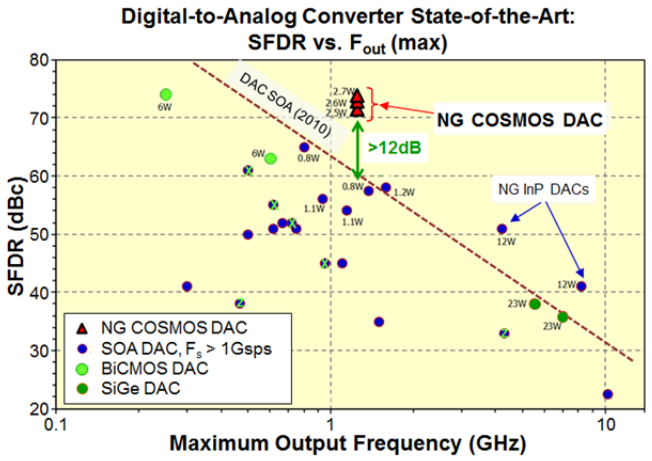

Figure 3: Plot of SFDR vs. maximum output frequency of state-of-the-art DACs. Northrop Grumman (NG) COSMOS data points are shown in red.

DARPA is also pursuing the integration of GaN transistors with Si CMOS on a Si substrate, and DAHI performers recently demonstrated a monolithically integrated RF amplifier circuit (see Figure 4 and Figure 5) using heterogeneously interconnected GaN HEMTs and pMOS gate bias control [15].

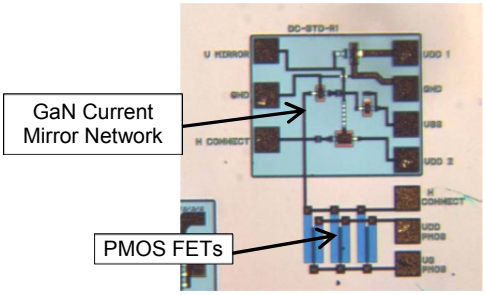

Figure 4: Optical micrograph of Raytheon/MIT's monolithic heterogeneously integrated GaN HEMT+CMOS RF power amplifier circuit (adapted from [15]).

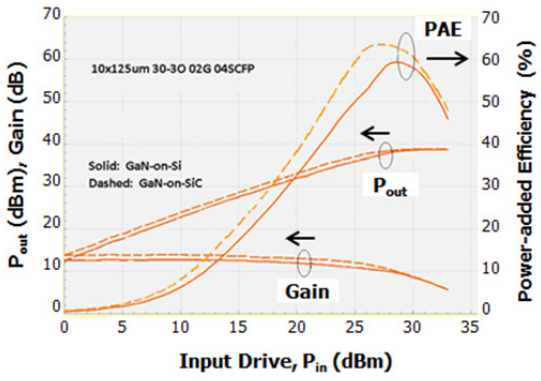

Figure 5: Representative microwave measurements at 10GHz for the GaN HEMTs shown in Figure 4 (solid lines), as well as control samples fabricated on SiC substrates (dashed lines) (adapted from [15]).

DAHI has also begun transferring COSMOS heterogeneous integration technology to a foundry manufacturing model. In the COSMOS multi-project wafer (MPW) thrust, InP BiCMOS technology is being utilized by a number of expert circuit design teams. The design teams have developed several innovative circuit designs which are expected to demonstrate the utility of heterogeneous integration for microwave communications, imaging, and remote sensing. The COSMOS MPW foundry team is using these multi-project wafer fabrication runs to systematically improve process control and yield while also refining the process design kit used by designers.

Meanwhile, the Electronic-Photonic Heterogeneous Integration (E-PHI) thrust was recently initiated as an element of DAHI. The goal of E-PHI is to enable novel chip-scale electronic-photonic/mixed-signal integrated circuits on a common silicon substrate which offer a considerable performance improvement and size reduction versus current, state-of-the-art technologies. This technology is expected to enable a wide range of novel chip-scale optoelectronic microsystems, including coherent optical systems for sensing (LADAR) and communications, optical arbitrary waveform generators, and multi-wavelength imagers with integrated image processing and readout circuitry. E-PHI will develop process and device technologies for heterogeneous integration (see Figure 6) as well as novel architectures for heterogeneously integrated electronic-photonic integrated systems. Finally, E-PHI plans to culminate in the demonstration of novel heterogeneously integrated electronic-photonic microsystems, including an ultra-low noise integrated semiconductor laser (see Figure 7.a) and an RF opto-electronic signal source with extremely low jitter (see Figure 7.b).

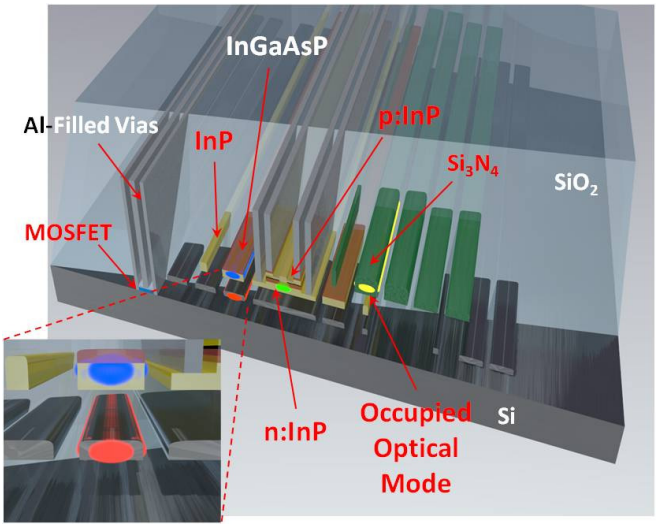

Figure 6: Conceptual drawing of electronic-photonic heterogeneous integration platform to be developed in DAHI. Image courtesy of S. Radic, Univ. of California – San Diego.

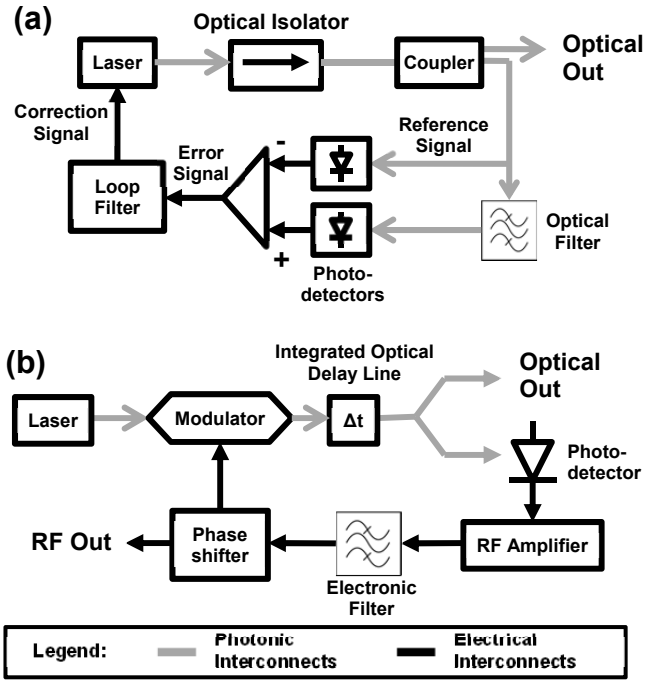

Figure 7: Representative block diagrams of E-PHI demonstration microsystems, (a) frequency-stabilized laser source, and (b) RF opto-electronic signal source.

In the future, it is anticipated that this expanded portfolio of heterogeneous integration technology modules will be available to designers through a high-yield, manufacturable DAHI foundry technology.

CONCLUSION

Device-scale heterogeneous integration holds considerable promise to enable novel advanced microsystems through the use of the best devices and materials for each function in an integrated system. Application areas include advanced RF/mixed signal electronics, integrated photonics, MEMS, as well as novel combinations of the above. The DAHI goal is to realize this promise through initiatives in process module development, innovative circuit design architectures and methodologies, and manufacturing. Results to date indicate that heterogeneous integration is both technologically possible and of significant value to high-performance military and commercial applications.

ACKNOWLEDGEMENTS

The authors would like to thank the following teams for their efforts in the COSMOS program: HRL Labs, Malibu, CA; Northrop Grumman Aerospace Systems, Redondo Beach, CA; and Raytheon, Andover, MA. The authors also thank design team participants in the COSMOS MPW initiative. The authors thank the participants in the E-PHI thrust, as follows: Aurrion, Inc., Goleta, CA; Massachusetts Institute of Technology, Cambridge, MA; the Univ. of California, Berkeley; and the Univ. of California, San Diego. The authors also thank the COSMOS, COSMOS MPW, and E-PHI US government agents for their support.

REFERENCES

[1] R. Lai, et al, "Fabrication of InP HEMT Devices with Extremely High Fmax", presented at the 2008 International Conference on Indium Phosphide and Related Materials, Versailles, France.

[2] S.E. Turner and D.E. Kotecki, "Direct Digital Synthesizer With Sine-Weighted DAC at 32-GHz Clock Frequency in InP DHBT Technology," *IEEE Journal of Solid-State Circuits*, Vol. 41, No. 10, Oct. 2006, pp. 2284-2290.

[3] Y.F. Wu; M. Moore, A. Saxler, T. Wisler, P. Parikh, "40W/mm Double Field Plated GaN HEMTs," *64th Device Research Conference*, 2006, pp. 151-152.

[4] Cree's Silicon Carbide Schottky Diode Chip CPW2-1200-S050B.

[5] C.-H. Jan, et al, "A 45nm Low Power System-On-Chip Technology with Dual Gate (Logic and I/O) High-k/Metal Gate Strained Silicon Transistors," *IEDM Tech. Dig*., pp. 637-640, 2008.

[6] Chevalier, P.; et al. "Towards THz SiGe HBTs," *2011 IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM)*, pp.57-65, 2011.

[7] Adrian Tang, et al. , "A Low Overhead Self-Healing Embedded System for Ensuring High Performance Yield and Long- Term Sustainability of a 60GHz 4Gbps Radio-on-a-Chip", *to be presented*, *2012 IEEE International Solid-State Circuits Conference (ISSCC)*, Feb 2012.

[8] E.O. Johnson, "Physical limitations on frequency and power parameters of transistors", *RCA Review*, vol. 26, pp163-177, 1965.

[9] E. L. Friedrich, M. G. Oberg, B. Broberg, S. Nilsson, and S. Valette, "Hybrid integration of Semiconductor Lasers with Si-based single-mode ridge waveguides," *J. Lightwave Technol*. 10, 336-340 (1992).

[10] M. C. Hargis, R. E. Carnahan, J. S. Brown, and N. M. Jokerst, "Epitaxial lift-off GaAs/AlGaAs metal-semiconductor-metal photodetectors with back passivation", *IEEE Photonics Technology Letters*, vol. 5, no. 10, 1993.

[11] Augusto Gutierrez-Aitken, , et al., "Advanced heterogeneous integration of InP HBT and CMOS Si technologies for high performance mixed signal applications," *IEEE Microwave Symposium Tech. Dig.*, pp. 1109-1112, 2009.

[12] T.E. Kazior, et al., "A high performance differential amplifier through the direct monolithic integration of InP HBTs and Si CMOS on silicon substrates," *IEEE Microwave Symposium Tech. Dig*., pp. 1113-1116, 2009.

[13] J.C. Li, et al., "Heterogeneous wafer-scale integration of 250nm, 300GHz InP DHBTs with a 130nm RF-CMOS technology," *IEDM Tech. Dig*., pp. 944-946, 2008.

[14] Augusto Gutierrez-Aitken, et al., "Advanced digital-to-analog converters using heterogeneous integration of InP HBT and CMOS Si technologies," *IEEE CSICS Symposium*, 2012 (in preparation).

[15] W. E. Hoke, et al. "Monolithic integration of silicon CMOS and GaN transistors in a current mirror circuit", *J. Vac. Sci. Tech. B 30(2)*, pp. 02B101-1-6, 2012.

ACRONYMS

CMOS: Complementary Metal-Oxide-Semiconductor
COSMOS: Compound Semiconductor Materials on Silicon
DAHI: Diverse Accessible Heterogeneous Integration
DARPA: Defense Advanced Research Projects Agency
E-PHI: Electronic-Photonic Heterogeneous Integration
HBT: heterojunction bipolar transistor
HEMT: high electron mobility transistor
LADAR: Laser Detection And Ranging
MEMS: Micro-Electro-Mechanical Systems
MPW: Multi-project wafer
SFDR: spurious-free dynamic range